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AlGaN/GaN HFETs fabricated on 100-mm GaN on silicon (1 1 1) substrates

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Abstract

The group III-nitride material system has been demonstrated by many groups to produce high performance, heterostructure field effect transistors (HFETs). AlGaN/GaN heterostructures yield high two-dimensional electron gas densities with high carrier mobilities and simultaneous high breakdown field. Devices based on this structure perform well at high power and at high frequency operating conditions. Most AlGaN/GaN HFETs to date have been produced on sapphire or silicon carbide substrates due to the limited availability of bulk GaN substrates. There are limitations in using these substrate materials in either thermal conductivity, cost or wafer diameter.

The use of silicon substrates can overcome the issues of sapphire and SiC that limit manufacturability. In this work, results from HFETs fabricated on 100-mm silicon substrates using a proprietary MOCVD reactor design will be presented.

The quality and uniformity of the GaN epitaxy, the microwave characterization of these devices at 2 GHz, and the thermal performance of large periphery devices on this material will be detailed. The electrical performance of these devices is found to be comparable to that of early devices on sapphire and SiC. The results will illustrate the viability of silicon as a low cost, manufacturable platform for AlGaN based devices from the standpoint of epitaxy, device performance, and thermal power handling.

1. Introduction

As wireless communications technology moves forward, the performance requirements placed upon the power amplifiers in these systems grow more difficult to meet. Currently, base station power amplifiers in these systems use silicon LDMOS transistors in the output power stage. As the limit of operability of these devices is reached, there will be a need for a semiconductor material that can fulfill the high frequency and high power requirements of the third generation of wireless technology.

Gallium nitride and its related alloys are widely acknowledged as a prime candidate for high power microwave applications due to their high breakdown field (3 MV/cm), high electron saturation velocity (2.5×10^7 cm/s), and high operating temperature. The associated heterostructure system, AlGaN/GaN, yields two-dimensional electron gases with high sheet charge concentration (in excess of 1×10^{13} cm^{-2}) and electron mobility (up to 2000 $cm^2/V\,s$), enhanced by the spontaneous and piezoelectric polarization present in the heterostructure [1,2]. The impressive electronic properties of these materials have been exploited in the form of HEMT structures to generate record output power densities up to the X- and Ku-bands [3,4].

Due to the limited availability of bulk GaN substrates, most AlGaN/GaN HEMTs to date have been grown heteroepitaxially on sapphire or SiC. Although impressive devices have been reported with both substrates, neither offers a clear commercialization pathway due to high cost, limited wafer diameter, and in the case of sapphire thermal performance.

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The Nitronex Corporation, founded in 1999, has developed a technology for growing GaN on 100-mm silicon substrates. A wafer fabrication facility has been built and a baseline fabrication process developed specifically for GaN device technology. The device design has been approached from the standpoint of high power device operation for power amplifier applications. The current state of this effort is reported here.

We will report on the development of GaN grown directly on silicon wafers. Using a transition layer scheme, which addresses both the thermal expansion and lattice mismatch in this material system, excellent epitaxial film quality has been demonstrated, as evidenced by 2DEG electron mobilities as large as 1800 cm^2/V s. These films are grown by MOCVD on 100-mm silicon substrates using a proprietary reactor design. Uniformity is typically within ±10% across the 100-mm wafer.

Using this novel GaN epitaxial technology as a baseline, an AlGaN/GaN HEMT process has been developed and the resulting devices characterized for microwave performance. Small periphery devices of 300 μm gate width exhibit saturated power densities as high as 1.6 W/mm. Characterizing devices with a 3 mm gate periphery, an output power of 3.2 W at 1 dB gain compression and saturated output power of 4.1 W with associated gain of 11.3 dB has been achieved.

A thermal model developed using a commercially available finite-element code has been developed. This model has been validated with infrared thermal imaging and is being used to thermally optimize the cell layout. Simulated and measured thermal results are in good agreement and indicate that the use of the silicon substrate does not present a significant thermal performance barrier.

Although AlGaN/GaN HEMTs grown on Si are promising devices for high power base-station transmitter applications at 2 GHz operation, Si substrate losses at higher frequencies may limit the gain and efficiency of these devices. In view of this, we present alternative approaches for extending the frequency response of this material system by taking advantage of commonly available silicon wafer bonding technology.

2. Epitaxial growth and material properties

A reactor design has been developed specifically for the growth of gallium nitride on 100-mm substrates. The reactor employs a vertical flow, cold wall design with high-speed substrate rotation. Using this reactor design, a transition layer scheme has been developed to accommodate the lattice and thermal mismatch of GaN to silicon. Finite element simulation has been used to improve the understanding of behavior within the growth reactor and to optimize the reactor design. A stable, reproducible growth process has been established which produces highly uniform, high quality, crack free GaN epilayers on silicon.

By combining the growth capabilities described above with readily available 100-mm silicon substrates, we have been able to achieve remarkable results in terms of uniformity across the wafer. Fig. 1(a) shows a typical thickness map of our 100-mm HFET process. The total

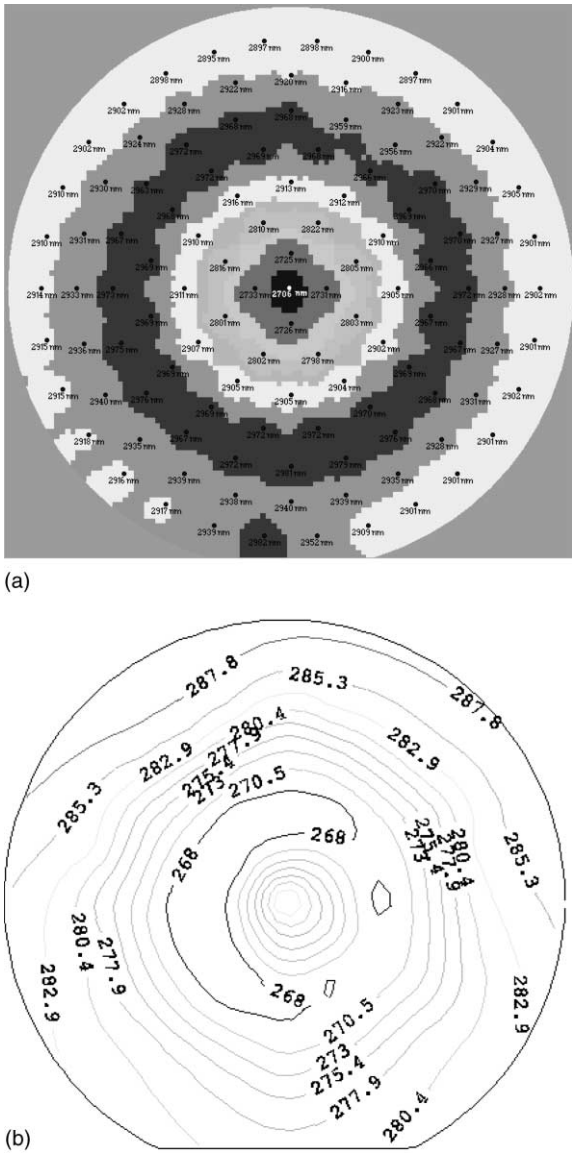

Fig. 1. (a) Filmetrics thickness map of an AlGaN/GaN HFET grown on 100-mm silicon. The average film thickness is 2.92 μm with a TTV of 9.4% and a standard deviation of 2.0%. (b) Lehighton sheet resistance map of an AlGaN/GaN HFET grown on 100-mm silicon. The average sheet resistance is 274 Ω/sq with a variation of 10.8% and a standard deviation of 6.6%.

epitaxial film thickness averages 2.92 μm across the wafer. The total thickness variation (TTV), calculated maximum minus minimum divided by the average, is less than 10% with a standard deviation of 2.0%. This figure represents the current Nitronex baseline HFET process. By further improvements in our process we have been able to achieve films with 1.9% TTV and a 1.1% standard deviation. This 'best' result represents the capabilities afforded us by the flow control available in the proprietary gas injection design.

The uniformity of the epilayers in not limited to layer thickness, but includes the electrical properties of the layers as is evident from Fig. 1(b) which shows a sheet resistance map taken using a Lehighton™ sheet resistance mapping system. The average sheet resistance across the 100-mm wafer is 274 Ω/sq (this includes parallel conduction in the silicon substrate) with a total variation of 10.8% and a standard deviation of 6.6%. The sheet resistance is an accurate measure of the charge and mobility in the 2DEG of the HFET (proportional to the inverse of sheet charge times mobility) and, thus gives a good representation of the Al composition and Si-doping concentration variation across the wafer. For comparison, we have taken multiple Hall electrical measurements across a 100-mm HFET wafer. The typical mobility and sheet carrier concentration is 1590 cm^2/Vs and 1.2×10^{13} cm^{-2}, respectively. The $N_s\mu$ product total variation across the wafer is 6.4%, which is in good agreement with the sheet resistance uniformity.

3. Device structure and layout

The device structure employed in the current work is shown in Fig. 2. This structure is similar to that employed by many other groups for fabricating AlGaN/GaN FETs. Growth was initiated on a Si(1 1 1) substrate using a transition layer scheme to overcome thermal expansion and lattice mismatch. A thick GaN layer was then grown, onto which the HFET structure is deposited. The HFET structure consists of an undoped AlGaN spacer layer of 50 Å, an AlGaN donor layer containing 2×10^{18} Si atoms, and undoped AlGaN followed by GaN cap layers. The aluminum mole fraction in all AlGaN layers was nominally 0.25. This conservative structure was chosen to insure reproducibility and uniformity of device performance, both across the wafer and from wafer to wafer.

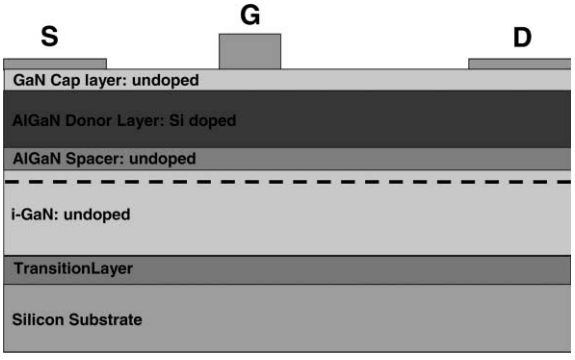

Fig. 2. Device structure of AlGaN/GaN HFET on silicon substrate.

A conservative device layout was employed for the same reasons as above. The layout was designed for high power operation at a frequency of 2 GHz. The nominal gate length was 1 μm, the source–gate spacing was 1 μm, and the gate–drain spacing was 3 μm for all devices reported in this work.

4. Device fabrication process

Devices were fabricated using a typical GaN liftoff based process, achieved with contact lithography techniques. Source and drain ohmic contacts were fabricated by evaporating Ti/Al/Ni/Au on a device structure patterned with a photolithographic lift-off process, then alloyed in a RTA for 30 s at 900 °C. Device isolation was achieved by dry etching of mesas in a RIE system that employs chlorine-based chemistry. The gate, Schottky contact, was also patterned for lift-off and consisted of evaporated Ni/Au layer. The active devices were passivated with a deposition of silicon nitride after the gate contacts were in place.

In order to connect the multiple fingers of large gate periphery devices, a plated air bridge process was employed. This process consists of a photolithography step to define the points of contact to the devices, a seed metal layer for the gold electroplating process, and a second photolithography step to define the regions to be plated. A 3-μm gold layer was plated onto all contact pads and as interconnects of multiple fingers of large devices. Finally, devices were encapsulated in benzocyclo-butene to prevent damage or shorting.

Devices of small periphery were characterized on wafer using a coplanar ground–signal–ground configuration. In order to characterize devices of larger gate periphery, wafers were thinned to enhance thermal extraction and then diced into chips. Chips were packaged into standard microwave packages using eutectic solder and connection was made from the pads on the chip to the packaged leads using gold wire bonds.

5. Electrical results

Electrical measurements were focused on two device geometries, a 300 μm coplanar structure and a 3 mm multifingered device, also of coplanar configuration.

Devices were measured at both DC and microwave operating conditions. Devices typically supported a saturated drain current of 850 mA/mm at $V_G = 0$ V, with maximum drain current of 975 mA/mm at $V_G = +1$ V. The transfer characteristics exhibited a peak g_m of 196 mS/mm.

For large signal microwave characterization of the devices on wafer, a Maury load-pull system was used. Output power sweeps of these devices were conducted at 2 GHz, the target operating frequency of these devices. The devices were biased to an operating point of $V_G = -1.5$ V and $V_D = 15$ V, which corresponds to class A operation. Source and load tuners were optimized to deliver maximum P_{out} with $P_{in} = 15$ dBm. The output power, power added efficiency, and gain as a function of input power for a device of 300 μm gate width are shown in Fig. 3(a). Output power at 1 dB gain compression, P_{1dB}, was 25.92 dBm at 12 dB gain, giving a power density of 1.3 W/mm. Peak PAE for this device was 24%. The data from a power sweep of a 3-mm device is shown in Fig. 3(b). A value of $P_{1dB} = 35.1$ dBm at a gain of 11.3 dB was observed, corresponding to a power density of 1.08 W/mm. Peak PAE for this device was 27%.

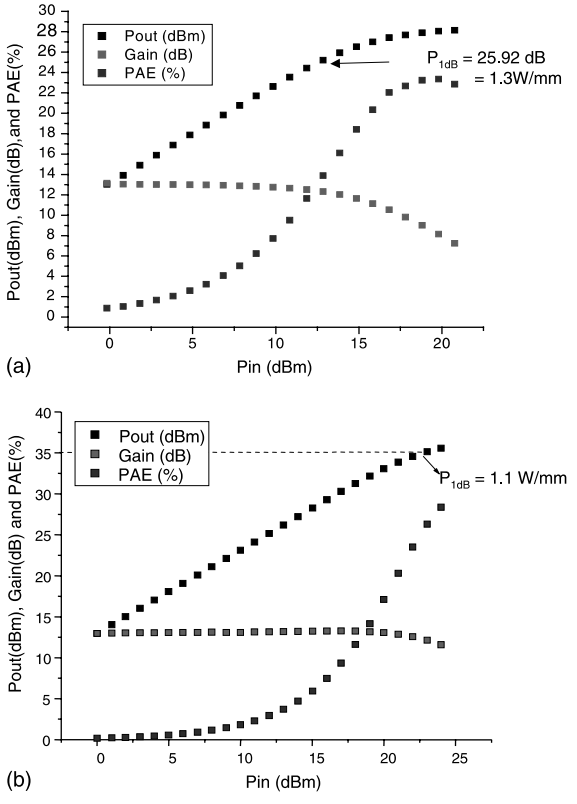

Fig. 3. Ouput power characteristics from (a) a 300 μm AlGaN/GaN HFET and (b) a 3 mm AlGaN/GaN HFET.

6. Thermal results

A numerical model was developed to predict the thermal power handling capability of the AlGaN/GaN based HFETs on silicon substrates. The heat conduction equation was solved in three dimensions, using commercial software from CFDRC. The model included a 1×3 mm chip consisting of a GaN epitaxial layer (2 μm) on a thinned silicon substrate (100 μm), packaged with eutectic solder (25 μm) into a CuW based microwave package (10 mm). The heat generation in the device was represented by planar heat sources of width 200 μm and length 1 μm located on the surface of the semiconductor. The thermal conductivities of GaN and silicon were given by polynomial expressions in order to account for their temperature dependent behavior.

In order to validate the results from the thermal model infrared thermal imaging was carried out at Quantum Focus Instruments. The IR microscope, the InfraScopeII provides emissivity compensation at every pixel and produces a complete thermal map. The temperature measurements are based on the intensity of infrared emission from the surface of the device. The intensity of this emission will depend on the emissivity of the materials at the surface and the temperature. It is possible to correct for the different emissivities by acquiring a map of the emission from the device held at known uniform temperature (80 °C). The device is then operated under DC conditions and the IR emission is measured again. Using this new measured emission and the stored emissivity map, the temperature of the device can be calculated. The InfraScopeII can obtain as good as 3 μm spatial resolution and 0.1 milliKelvin accuracy [5].

Measurements were carried out on eight devices at conditions from 1 to 8 W of DC power. The tested devices consisted of three different gate pitches (25, 35, and 45 μm) and three different gate finger widths (100, 200, 300 μm) with all devices having 10 fingers. Table 1 summarizes the results of these measurements. Peak temperature depends as expected on the geometry of the chip. The observed increase in thermal resistance, R_{th}, with increased power is attributed to the inverse relationship of thermal conductivity with temperature.

The measured results show good agreement with the simulation results as illustrated in Fig. 4, which shows junction to case temperature rise vs. DC power for four devices and the simulation. The device which appears hotter than the others is believed to have a poor die attach, limiting the heat transfer from the chip.

The results confirm the expected effects of changing gate pitch and width. Furthermore, we now have a quantifiable measure of this effect, which can be taken into account during design. The agreement between simulation results and experiment give confidence to the use of the simulation results for optimizing device layout.

Table 1
Calculated thermal resistance of packaged chips based on measured values of peak temperature

Gate pitch (μm)	Gate finger width (μm)	R_{th} (°C mm/W)
25	200	47.08 (average of four devices)
35	200	37.26
45	200	32.16
25	100	25.79
25	300	55.80

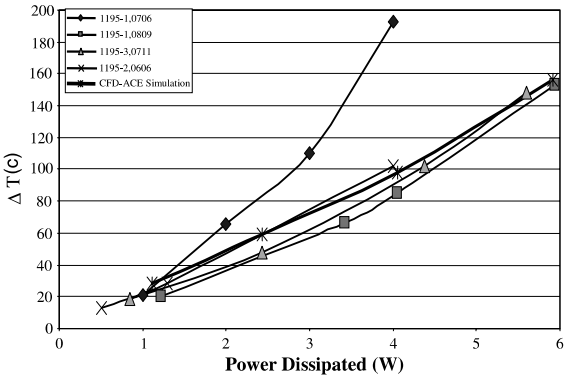

Fig. 4. Junction temperature rise as a function of dissipated power from measured devices and simulation results.

7. Conclusions

The capability to grow high quality GaN epilayers on 100-mm silicon substrates has been demonstrated. Results show a high degree of uniformity on a wafer scale. AlGaN/GaN heterostructure FETs have been grown and fabricated on these wafers. Characterization of these devices shows promise for high power operation, with current output power being as high as 1.6 W/mm. No fundamental barrier to improving power density of these devices has been observed. Efforts will continue in optimizing the device structure and layout to improve performance.

Simulation and measurements of the thermal performance of these devices indicate that silicon is a viable substrate for high power devices, providing adequate heat sinking capability for the power density required for the targeted wireless applications.

Although HFETs perform well on silicon at 2 GHz, it is anticipated that a reduction in substrate conductivity will be required above X-band. There are a number of options available to be coupled with technology of GaN on silicon. It is possible to take advantage of existing silicon wafer bonding technology and incorporate for example, a polycrystalline AlN substrate which would serve two roles: reducing the thermal impedance of the chip and providing a highly resistive substrate to allow operation at higher microwave frequencies. Further options include flip chip packaging for RFICs, or with the appropriate substrate even GaN based MMICs. In conclusion, GaN on silicon offers a viable, cost effective alternative to the commercialization of AlGaN/GaN HEMTs in high power microwave applications with the ability to extend operation to higher frequency bands.

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