Volume Epitaxial Growth of Enhanced Mode HIGFETs using Minimal Material Characterization and Rapid Inline Processing to Minimize Risk

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Abstract

Previously, our epi-manufacturing group has reported on the growth of enhancement mode HIGFETs for cell phone applications [1]. Since that report two Emcore E-450 Turbo-Disk reactors have been installed capable of 5x6-inch growth. Both reactors are qualified to run the HIGFET product with a combined maximum average output of between 900-1000 wafers/week. The original single wafer epitaxial growth tool output was about 150 HIGFET wafers/week. There is a significant possibility of increased scrap events from improper epi due to the increased output of the two reactors, the difficulty in projecting the device electrical parameters from the finished epi, and the length of time between insertion in the line and initial test results. Our enhanced mode HIGFET structure (EMODE) is a fully depleted structure [2, 3] and does not lend itself to many standard production-oriented characterization techniques. Typically, one would use Hall, photoluminescence (PL) [4], and/or x-ray measurements to analyze this type of structure (with higher grown-in charge). These methods have limited correlation in this case [5]. Therefore, to minimize risk, we have developed a basic set of non-destructive characterization tools and coupled it with rapid processing to get initial electrical data. We use a Lehighton measurement coupled with a PL measurement as a pass/fail test after growth. The range and value of the Lehighton measurement can give us information about the charge level in the epi structure in general. We can then use the full-width-at-half-max value of the PL spectra to get information about the amount of the charge in the channel region. In this way we can tell the amount and general location of charge in the structure. Neither test is sufficiently accurate to measure electrical performance absolutely, but is instead useful as a go-no-go to the next step. Once the wafers pass the initial testing they are put into the process line. Rapid in-line results are obtained in four days, which give initial electrical parameter results. Based on these electrical results the wafers are qualified or downgraded.

INTRODUCTION

CS-1 provides enhancement mode HIGFETs (EMODE) for cell phone power amplifier modules in the United States and Europe. The device is a characterized by having high power and power added efficiency and low off-state leakage, which leads to less required circuitry, and longer battery life due to a single power supply to drive the device.

The EMODE device is a depleted structure that is not easily characterized by typical production worthy techniques. Physically, one can determine layer thickness by TEM destructively or generally by high-resolution x-ray methods. The sheet resistance of the epitaxial layers can be measured, but is effectively infinite so that little data except a first order check of the correctness of the layers and doping can be determined. Typically, end of growth monitoring for the EMODE process has consisted of a contactless sheet resistance measurement and a general monitoring of the PL and x-ray characteristics. The wafers are then run in the process line and electrical results for threshold voltage, off-state leakage and other device parameters are obtained before it was known if the growths are good or not.

In the single wafer epitaxial growth system previously employed we were able to process and characterize wafers so that the associated risk was held at about 85 total wafers. As production numbers have risen and device requirements have become more stringent the requirement to know if the wafers are ‘good’ or not has become more urgent especially considering the number of wafers at risk could be as high as 1000. In response, a known good epi (KGE) flow has been developed by the epi group. This flow generally consists of characterizing incoming substrates, growing epi on the wafers, characterizing the as-grown epi, fabricating devices on a sampling from the characterized ‘good’ epi (while holding the balance), and either releasing or scrapping the held wafers based on results of the in-line electrical characterization.

METHOD

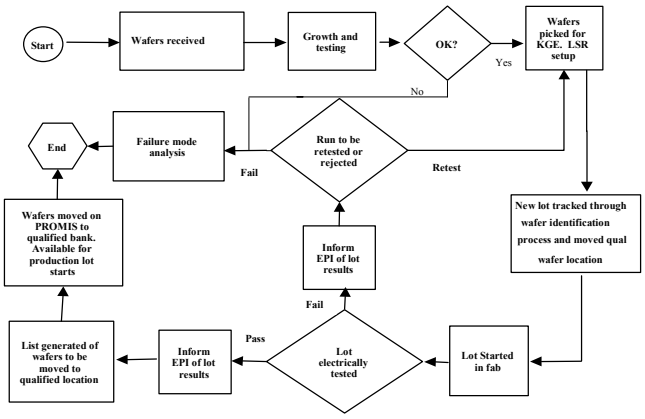

Figure 1 – CS-1 internal EMODE flow.

The KGE process flow is shown in figure 1. The process is divided into four basic parts. First, incoming wafers are inspected and rejected or accepted and formed into parent lots. Second, the EMODE growth process is run and characterized. The runs are tested 100% for sheet resistance and particles and one wafer per run for x-ray and PL information. The data for the sheet resistance and the particles is trended while the data for PL and x-ray is qualitative and is held for comparative information. Third, based on the characterization data the runs are sampled (currently) at the rate of one wafer every other run. These sampled wafers are split into test lots (KGE lots) and started in the process line. The associated wafers are held. Finally, the in-line electrical data is collected and used to determine the 'goodness' or 'badness' of the epi. Wafers that are found to pass in all aspects are sent on, and all associated runs are accepted as known good epi. Failure mode analysis is done on all partially or totally failing wafers. Based on root cause the wafers are rejected, with all associated wafers scrapped, tested again (for verification), or accepted as KGE. The end result is that wafers that pass KGE are ultimately shipped as product to our customers.

CHARACTERIZATION

The primary end of growth characterization is for sheet resistance and particles. We also monitor the PL and x-ray information due to previous work by Brierly and CS-1 [6]. It has been shown that for pHEMTs it is possible to measure and quantify the epitaxial growth by using the PL line shape and spectral content. CS-1 is attempting to carry this over to the EMODE structure.

Sheet Resistance - The most consistent data collected after epi but before process is for sheet resistance. Table 1 shows the criteria for acceptance of the epi based on this test. The data is useful in the following manner. For high values of sheet resistance (> 90,000 ohm/sq) the wafers are assumed to be good and sent on for other testing. For values between 60,000 and 90,000 ohm/sq the wafers are suspect. In this case they are flagged and started in KGE lots. If the sheet resistance of all wafers in a run is less than 60,000 ohm/sq the wafers are quarantined.

TABLE 1
Sheet resistance key

Sheet Rho (ohm/sq)	Result
> 90,000	Pass
60,000 – 90,000	Pass but flagged
All wafers < 60,000	Failed

The limits in Table 1 have been derived from experimental and production data. For instance, in one circumstance where the buffer material was doped the effect was to shift the sheet resistance value without changing the apparent threshold. In that case it was useful to use the PL data in concert with the sheet resistance information to determine information about the structure. This will be rediscussed later on in this section.

Photoluminescence - PL is done on one wafer per run and the line shape is confirmed as well as the fwhm value versus historical line shape and historical fwhm data. Figure 2 shows a plot of normalized threshold voltage versus fwhm. For these data $R^2 = .03$ and is not a good fit. It is likely that one reason for the low correlation is process variation. The data is generally consistent within a lot however. The fwhm is useful in a couple of cases. First, for the case of grossly incorrect doping in the channel CS-1 has performed corners experiments that

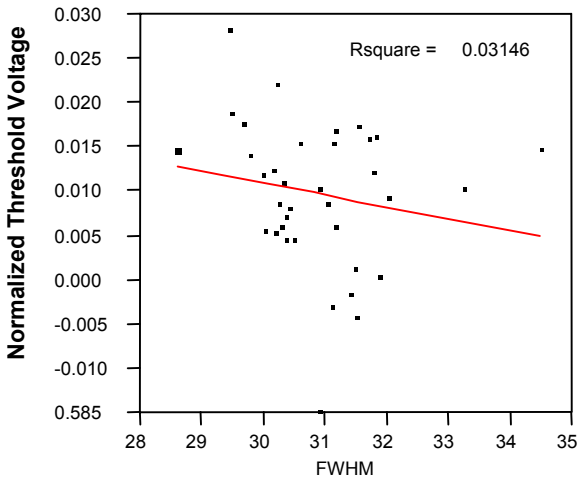

Figure 2 – Plot of threshold voltage versus full-width-at-half-maximum for EMODE2 wafers after growth but before process.

show a significant shift in the fwhm values for doping levels above and below the target. Figure 3 shows an overlay plot of two growths with a threshold shift of about 20 mV. One can see that as the fwhm increases the threshold voltage decreases.

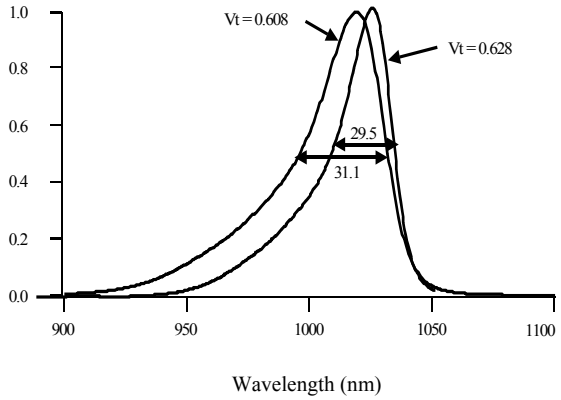

Figure 3 –Overlay of two growths showing change in FWHM Vs threshold.

Second, taking into account shifts based on gross changes due to excessive or too little charge the data in Figure 2 above shows that for a fwhm range of about 29-33 sec^{-1} the threshold voltage is generally shifts by about 25 mV. So in light of this information we use this measurement as a loose guide. If the data falls far below or above the range for fwhm, or the fwhm changes within run or run-to-run appreciably the wafers are flagged for a closer look. Otherwise the wafers are passed on to the next step.

As commented on while discussing the sheet resistance limits above, it is useful to look at the sheet resistance measurement and the PL data together to understand the charge in the epi structure. The PL measurement only measures excess charge in the vicinity of the channel [6] while the sheet resistance measurement measures the charge in the whole device. Therefore, if a sheet resistance

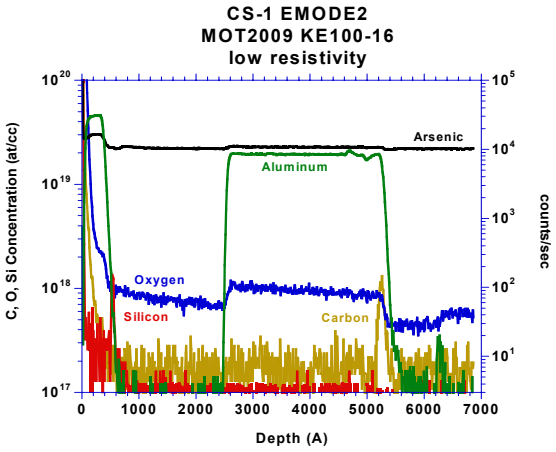

Figure 4 – SIMS data for a sample with a carbon pulse at the start of the buffer. Vt = 680 mV, FWHM = 30.8 sec-1. Sheet rho = 37,737 ohm/sq.

measurement is out-of-spec but the PL data looks good we conclude that there is varying charge in the structure either in the gate material or in the buffer. Figure 4 shows a SIMS sample of charge added at the start of the buffer. In this case the sheet resistance is 37,737 ohm/sq and the fwhm is 30.8 sec^{-1}. While the FWHM data is good based on our model the threshold voltage is high. The only indicator of this is the low sheet resistance measurement.

X-ray – X-ray testing is done to confirm the general spectral shape. The InGaAs is visible in the spectrum as well as the buffer AlGaAs composition. Due to the resolution of our current x-ray system the thickness information for the

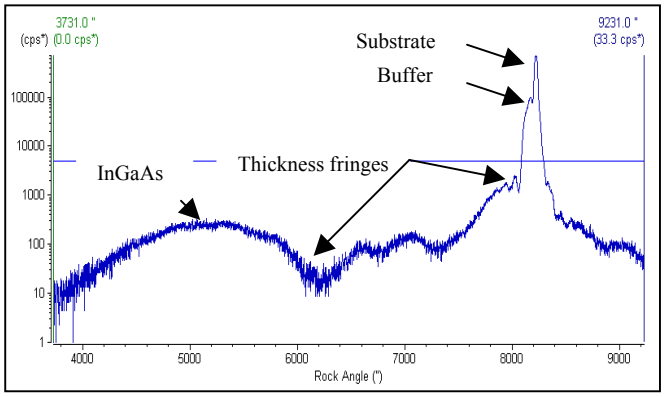

Figure 5– EMODE x-ray spectrum showing detail of the InGaAs channel and buffer.

various layers isn't accurate. Experiments have shown that x-ray methods for this device are not reliable as a source of exact measurements of thickness in particular, and instead trends can be indicated where layers are thin or thick. Figure 5 shows a typical x-ray spectrum. The noise in this measurement is apparent. We have recently taken delivery of a new tool that is capable of higher resolution measurements. We hope to have it qualified and part of the production measurement system by Q2 2003.

INLINE TEST RESULTS - Test results that confirm good epi include acceptable data for threshold voltage, off-state leakage and N+ and N- sheet resistance. Typically, once the KGE lots run through the inline tests a device engineer reviews the data. If the wafers pass they are send on. If the wafers fail the lot is held and examined for errors in measurement. If no measurement errors are found the lot is examined for growth or processing errors. Failing wafers are scrapped and used as test wafers for the factory. Figures 6a and 6b show examples of acceptable inline results for threshold and off-state leakage.

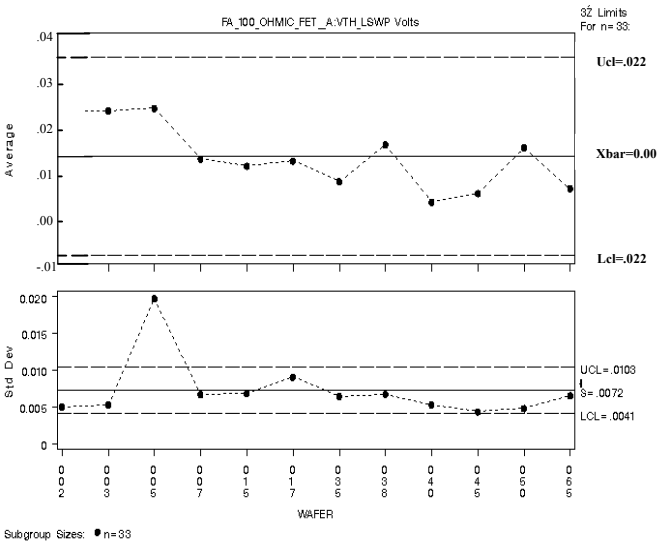

Figure 6a – good data for threshold voltage.

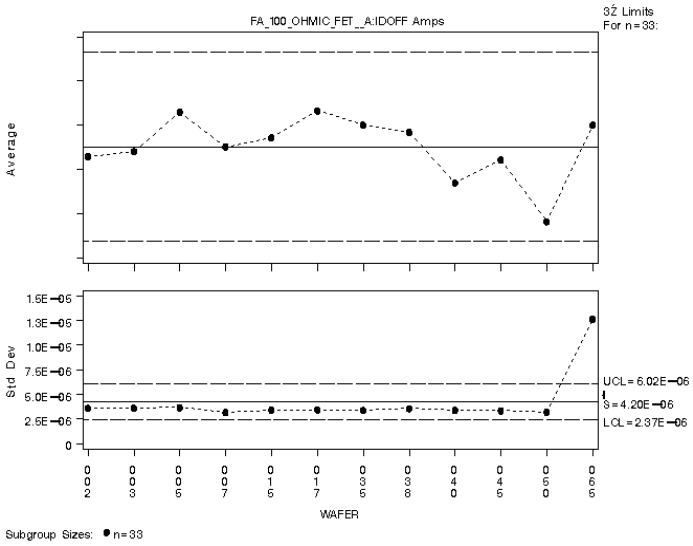

Figure 6b – good data for leakage current.

SUMMARY/CONCLUSION

Ultimately the best test as to the success of the process is the ability to hold the target parameters over the long haul, the reduction of scrap and reduction in cost. Figure 7 shows threshold voltage for over 250 runs. The specification window is 100 mV wide and the target is centered in that window. These runs covered a span of slightly less than 3 weeks. With the exception of the single point we are inside the derived control limits and always within specification. We have also reduced scrap by a factor of approximately 4 using this technique. Being able to react quickly to fluctuations has allowed us a significant advantage. Having a reliable internal source of epi wafers has allowed Motorola to rely more heavily on its internal wafer foundry and keep the costs associated with wafer growth low.

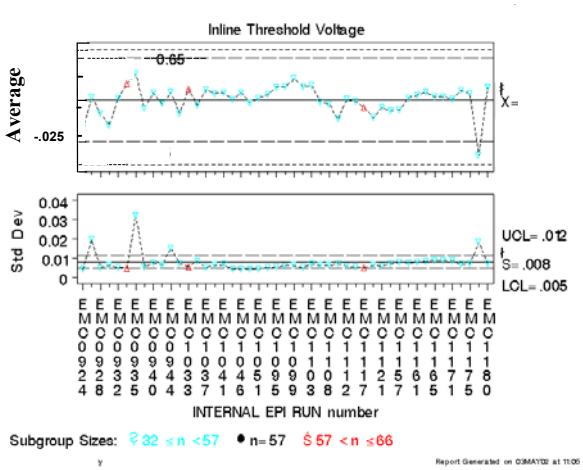

Figure 7 - shows threshold voltage data for 256 runs.

Finally, this process has worked to help keep us competitive with current wafer costs significantly less than those of our external suppliers.

CS-1 has developed a method for supplying rapid feedback on characteristics of epi and device electrical parameters to insure high yields to the wafer factory. Additionally, we have been able to reduce scrap, improve control and reduce wafer cost to benchmark levels.

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