



# *Applications of Contactless Sheet Resistance Probes to Achieve Cost Savings*

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## **Abstract**

Contactless eddy current measurements and maps are being used to monitor wafer manufacturing process and are helping to improve yields. Examples of applications to GaAs wafer are given, including one by a production user who has saved over \$250,000 per year. R & D small volume users have also achieved savings.

## **Introduction**

It is especially important to detect undesirable sheet resistance variations in incoming epitaxial or ion implanted and annealed wafers early, before adding the expensive process steps required to produce FET, PHEMT and HBT integrated circuits.

Since Lehightron became involved with the Electrical Properties Task Force of the SEMI GaAs Committee - now the SEMI Compound Semiconductor Committee - at its inception, its first responsibility was to gather feedback on the electrical properties of GaAs wafers from world users and producers. Having received excellent cooperation from these survey participants, we have been working with and reporting on non-destructive instrumentation methods that show promise in achieving a good correlation between material electrical property measurements and device performance parameters. Many of the following applications have helped customers to save hundreds of thousands of dollars. Most of the reports here are from papers presented by our users, while others come from those considering the purchase of instruments to improve their repeatability and capability. Some of the methods can be applied to silicon and conductive substrates with proper consideration. The contactless wafer sheet resistance probes are based on a paper [1] and patent by Miller et al. of Bell Labs. These employ a special marginal oscillator with the wafer placed between the upper and lower halves of the coil. The electronics and mechanics of the probes have evolved greatly in the six generations since our original Model 1000 was sold to Hewlett-Packard Santa Rosa in 1977.

From the start of development in 1976, we have used NBS (now NIST) silicon reference material wafers (SRMs) for calibration purposes. These have been extremely helpful in establishing the absolute values needed to maximize instrument performances and settle disputes. At times NIST SRMs have not been available, and have been substituted with wafers from commercial sources. These substitutions may result in yield problems and disagreements regarding absolute value differences. Any inputs that can aid in the definition of procedures and methods that should be used to assure adequate control and auditing will be appreciated. The new 100 mm NIST SRMs will start to be available in the last quarter of 1996.



The University of Illinois is helping with the correlation between measurements made on the Model 1310 probe using different mapping plans to determine the ability to resolve microinch defects in wafers. This will aid in determining and minimizing the eddy current measurement area, to enable an ASTM test method for eddy current sheet resistance mapping. The university will also provide a calibration standard of approximately 20,000 ohms per square to be used as an in-house standard.

The non-destructive sheet resistance measurement requires no fabrication steps, unlike the alternative procedures of point probe Isat measurements, the results of which have been compared closely with those of the present technique. Dr R.H. Wallis of GEC-Marconi Materials Technology Ltd states [2] that:

*"At GMMT active device areas were defined by implant isolation and then pairs of ohmic contacts (which eventually form the source and drain contacts of the transistor) were deposited. The saturated current (Isat) between each pair of contacts was probed over the wafer using an in-house automated test system. The correlation is very good, both maps showing a similar "bull's-eye" pattern slightly offset from the centre of the wafer. The uniformity (expressed as the standard deviation over the mean) of the two sets of measurements was also in good agreement."*

Daniel H. Rosenblatt, of National Semiconductor, formerly of Samsung Microwave Semiconductor, in this excerpt from his MANTECH paper [3], compares the eddy current probe with a commercially available GaAs four point probe for accuracy and precision.

The precision study was done by studying the "discriminating power" of the two instruments. The discriminating power of an instrument is its ability to differentiate between different pieces of product (in this case 24 measurement locations on the same wafer) by making multiple measurements on each piece and studying the range of measurement error. Discriminating power is defined in detail in the AT&T Statistical Quality Control Handbook. The comparison results showed that in respect to the application of the eddy current probe to MMIC yield enhancement the eddy current probe is the more precise and accurate sheet resistance probe. It is more suitable for yield enhancement applications where a variation in implantation dose, substrate donor or acceptor level, anneal furnace temperature, or other process variation must be detected to improve yield. In fact, the eddy current probe was used to measure blanket (unpatterned) channel implants into substrates from various suppliers. The probe determined that substrates manufactured by Supplier A produced a factor of two better across-wafer uniformity in sheet resistance than substrates manufactured by Supplier B. A total of 191 MMIC wafers were then fabricated on wafers from both suppliers. Each MMIC wafer had nine van der Pauw structures located across it for the determination of the channel layer sheet resistance and its uniformity. The sheet resistance for this channel layer is approximately 600 ohms/square.

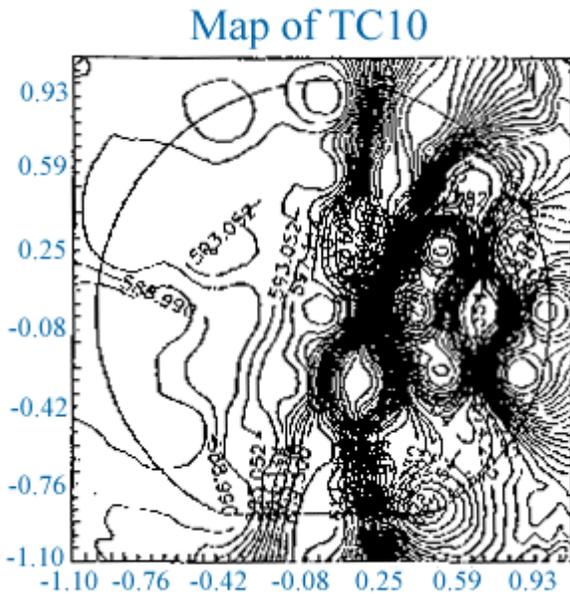
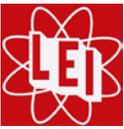


Figure 1: Sheet Resistance map of wafer hard spray rinse

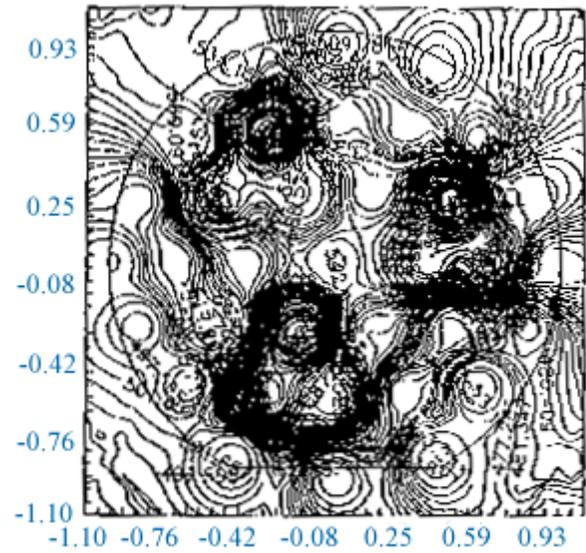


Figure 2: Sheet resistance map of wafer, showing (3) severe spots due to plasma machine

The median standard deviation was 14 and 31 ohms/square for Supplier A and B substrates, respectively. MMIC yield on Supplier A substrates was higher, in agreement with the eddy current probe and van der Pauw structure measurements.

## Ion Implant and Anneal Applications

The following quotation [4] from Dr Martin Brophy of TriQuint describes an application in which a contactless sheet resistance probe has helped save a customer over \$250,000 yearly:

*"Expedient utilization of measurements are used to qualify the important steps of the ion implant process detecting unwanted contamination in CVD processes and non uniform cleaning and etching. This has saved TriQuint more than \$250,000 per year by helping increase yields. Every day, a normal semi-insulating GaAs wafer is sent through our production front end, consisting of wafer prep, cap deposition, blanket FET channel implant and rapid thermal anneal. The wafer is then tested on the Leighton 1310 using a 35 point map. If the average sheet resistance and on-wafer uniformity fall within their SPC limits, the front end of the process is considered OK and the day's fab runs can be started. Otherwise, the front end is shut down for production and we mobilize to determine the source of the discrepancy and ameliorate it."*

The maps are an integral part of these savings. They reveal an uneven hard spray rinse (Figure 1) and three severe spots after processing in a plasma machine, showing a detectable contamination signature (Figure 2).



Further, Brophy says [4], *"In addition to production use, our Leighton systems are also widely used for rapid process development in implant and anneal and for potential new substrate suppliers."*

The following excerpts are from papers presented by some of our current and prospective customers at GaAs symposia. They state how the eddy current sheet resistance measurements have improved their process and yields.

Wilson et al., of Motorola Semiconductor Products Sector, Tempe, AZ, report [5] that

*"to address the difficult task of low dose ion implant monitoring for GaAs we have developed a technique that is very simple and elegant, but which is highly accurate for monitoring implant matching as well as absolute dose control. We dedicate an entire boule (typically greater than 150 wafers) for ion implanter monitoring. When the implanter is in a known qualified state, we utilize custom fixtures to implant one half of all wafers with Be and Si doses that are typical of our channel implants."*



**Figure 3: Sheet resistance map of wafer implanted with Si ion doses of 8.0 ( $10^{12}/\text{cm}^2$  at 135keV)**

**Figure 4: Sheet resistance map of wafer implanted with Si ion doses of 3.5 ( $10^{12}/\text{cm}^2$  at 140keV)**

This ‘standard implant’ is always performed on the same implanter, and becomes the reference implant. Twice per week on all implanters and whenever a source change is required, the other side of one of these wafers is implanted with the same Be and Si dose as the standard side. Subsequently, the wafer is annealed, contactless sheet resistance measurements are made, and the delta in sheet resistance between the standard and test side of the wafer is monitored. Our gage sensitivity tests of this monitoring technique have shown that it can accurately detect activated dose errors less than 0.5% which is well within the specifications of typical production ion implantation equipment. This technique has greatly enhanced our ability to detect machine problems that cause minor dose perturbations, and which otherwise would have gone undetected. We have devised similar techniques for monitoring absolute temperature, and matching for our rapid thermal annealing equipment. A



dedicated boule is implanted with a Si implant dose that ensures dose saturation in the GaAs substrate. This results in the activated sheet resistance being a function of the anneal temperature, and not small variations in the implant itself. We have determined that this monitoring technique gives us a sensitivity of 1 ohm/°C. In general, this sensitivity provides capability to ensure temperature repeatability of  $\pm 3^\circ\text{C}$ .

### **Brophy et al. write [6] that**

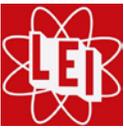
The implant activation was first studied for a number of commercially available GaAs wafers from different boules grown by both VGF and LEC technique. The substrates were blanket implanted at Raytheon and TriQuint, in both cases through a dielectric cap. The resulting sheet resistance values and uniformity were measured with Lehigh contactless conductivity probes at Raytheon and TriQuint.

The main focus of the study is on the evaluation of performance of E-FETs and D-FETs fabricated on VGF and LEC substrates. The FETs were produced in routine fabrication runs of TriQuint's QED/A process. That process is TriQuint's most popular process and features 1  $\mu\text{m}$  gate length recessed-gate D- and E-FETs.

Sheet resistance mappings were made of typical 100 mm VGF substrates after Si implantation and rapid thermal annealing performed at Raytheon and TriQuint. The sheet resistance measured by the Lehigh contactless conductivity probe is (332 ohm/sq. [Figure 3] and 840 ohm/sq. [Figure 4] for  $^{29}\text{Si}$ -ion doses and energies of 8.0 (1012/cm<sup>2</sup>) at 135 keV and 3.5 (1012/cm<sup>2</sup>) at 140 keV at Raytheon and TriQuint, respectively. These sheet resistance values are comparable to those that can be achieved by LEC substrates, and within the specifications of these two companies. The uniformity is observed to be excellent. Typical standard deviation of sheet resistance after ion implantation and rapid thermal annealing is only on the order of 0.5-1%. This is also comparable to, or sometimes better than LEC substrates.

A low energy implant (85 keV) at Raytheon showed that the implant activation on VGF substrates can be 5-10% lower than on LEC wafers. However, further investigations show that the lower activation can be readily offset by slightly adjusting the implant dosage. This yields consistent results both for sheet resistance and uniformity.

Slightly lower implant activation and consequently higher sheet resistance was observed at TriQuint on some blanket implants of VGF substrates. However, E- and D-FET devices were all fabricated without any adjustment of implantation conditions. In one case where sheet resistance was higher (opposite to the trend just mentioned) for the LEC substrates, a recess etch adjustment was used to achieve comparable FETs. Overall, no inferior device performance related to the slightly lower implant activation for VGF substrates in some blanket implants has been observed. It can even be seen that VGF substrates yield better device properties and tighter parameter distributions in some test runs.



## Epitaxial Wafer Applications

Brophy says [4], "For our HEMT production, one instrument is used for incoming inspection of GaAs epi wafers with sheet resistances of 30k ohm/square or higher. In that case we use the Leighton system to clear wafers for use." Work is continuing to enable better repeatability at these high sheet resistances.

Contactless sheet resistance measurement has been used to improve threshold voltage control. Lin et al., of Hewlett-Packard Labs, Palo Alto, CA state [7] that: Reproducible MBE growth of epi-layers and a uniform and reproducible RIE process have resulted in excellent threshold voltage (VTH) control. This was achieved using three techniques: daily flux measurements of the group III sources, calibration wafer growths before MODFET IC wafer lots, and individual screening of wafers. The wafer screening is accomplished with a non-contact resistivity monitor which allows the overall sheet resistance of the as-grown material to be measured with a repeatability of  $\pm 2\%$  over approx. 270 to 330 ohms per square.

(Note that the LEI 1310 1 sigma repeatability over this range is  $\pm 0.05\%$ .)

Beckham et al., of Emcore, show a sheet resistivity map (Figure 5) for a double planar doped p-HEMT wafer with a thin, lightly doped cap, showing a uniformity of better than 1.6% (1 sigma) [8].

## Monitoring Subsurface Damage due to Wafer Sawing and Polishing

In the MIMIC programme, Westinghouse, AvanteK, Rockwell, and TRW have used sheet resistance and conductance diameter scans (Figure 6), correlated with photon backscatter (PBS) red and blue wafers, in order to minimize subsurface damage caused by sawing and polishing, as well as to control the etching used to remove damage [9]. Figure 7 shows the effect of pre-implantation surface treatment on the sheet conductance of Si implanted, 3 inch diameter GaAs wafers after PSG capping and 830°C/30 s furnace annealing.

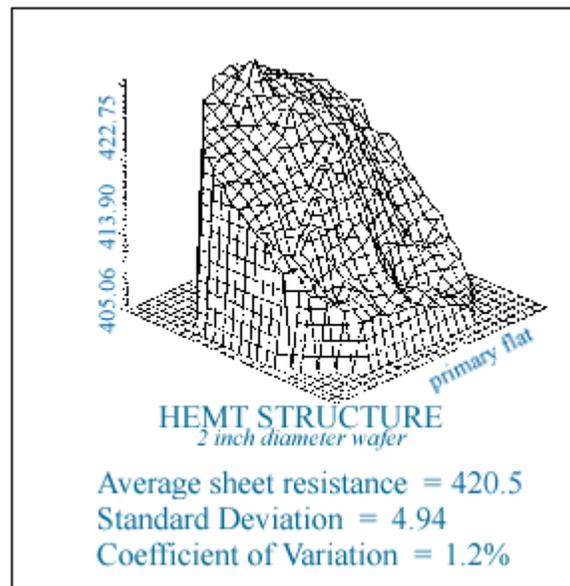


Figure 5: Sheet resistivity map for a double planar doped p-HEMT wafer

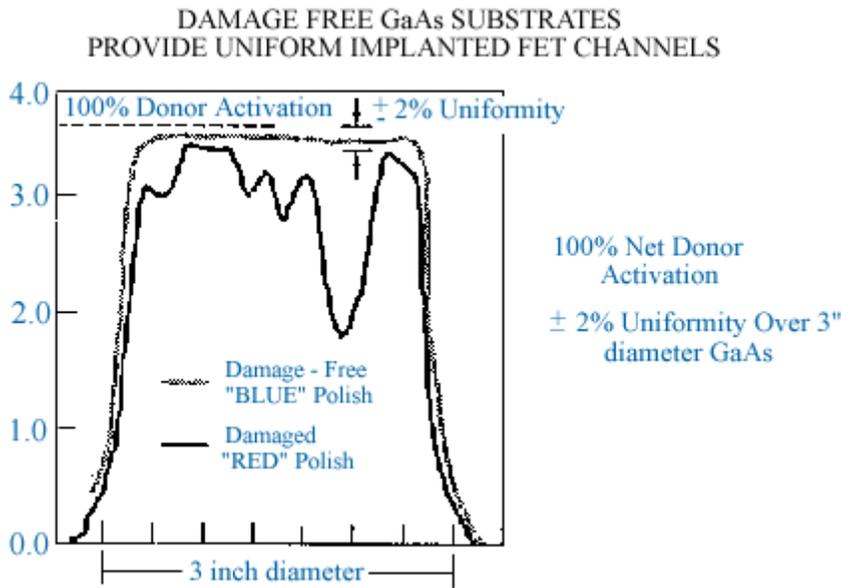
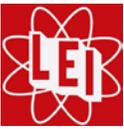


Figure 6: Sheet conductance diagram scans

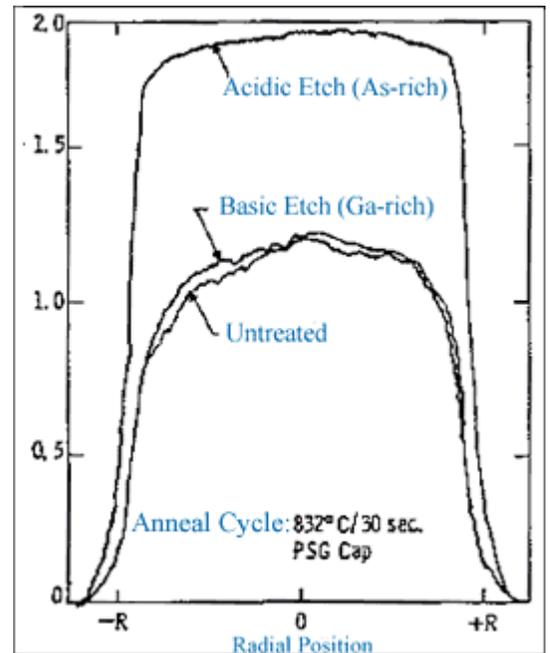


Figure 7: Effect of pre-implantation surface treatment on sheet conductance

## Reactor Test

Sheet resistance measurements and maps have been used by Aixtron, Emcore, and Riber to ensure that the epitaxial reactors are performing uniformly before sale and shipping. Tompa et al., of Emcore, show that, after growth parameter optimization, commercial III-V MOCVD production scale growth systems are capable of providing cross-sectional uniformity equivalent to that achieved by MBE [10].

CDV, Hall effect, PL, X-ray diffraction and contactless sheet resistance probe measurements were used to evaluate the doping and compositional uniformity of a variety of structures. Figure 8 shows a sheet resistivity map of a HEMT structure. The surface map is generated from a 55 point sampling pattern. The coefficient of variation for this wafer is 1.2%.

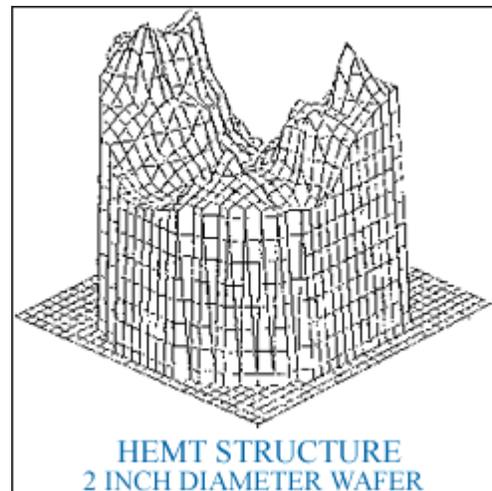
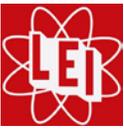


Figure 8: Sheet resistivity maps of HEMT structure



## **Cross-Check and Mobility Measurement**

The sheet resistance measurement capability of the LEI Model 1400 EMA mobility instrument enables a cross-check against the non-destructive sheet resistance mapping instrument. The mobility instrument, which is based on an invention at IBM Watson Research Center by Dr Norman Braslau, with improvements during and after the Ben Franklin Program at Wilkes University, enables non-destructive mobility measurements on production wafers. Feedback from Litton from their use of the instrument during and after their MIMIC programme has been used to enable measurement of the 2DEG mobility.

## **Metallization Monitoring**

An instrument with three-range (high, low, extra-low) capability provides for measurements of films ranging from Ni thin films with high sheet resistance to interconnect metallizations (Ti, Pt, Au) with very low sheet resistance. The non-contact RF measurement eliminates four-point damage and metal contamination from the points and enables measurement through oxides and coatings. Since there are no points to lower and raise during multi-point measurements, the measurement time for a 55 point plan can be as fast as 3.5 minutes, with improvements being implemented.

Measurements may be made on structured and patterned wafers and materials with grain boundaries without concern for where the points land. Very repeatable measurements have been made on 200 mm silicon wafers with poly, SiO<sub>2</sub>, Si T, Al, and WSi thin films. In-line measurements (load lock) may be made for immediate feedback and correction of thin film deposition before removing the wafer to room atmosphere.

## **Financing**

It should be understood that the cost savings mentioned above were realized in a production environment. Research and development applications with smaller quantities have reported savings of over \$30,000, based on the detection of substandard epitaxial wafers before additional (and expensive) labour and materials have been added. These potential savings, combined with our records which show that most purchases require a six-month to one-year minimum waiting period, can result in interim losses of \$100,000 - \$750,000 in terms of possible yield improvements. It is our hope that a "win-win" situation can be achieved, whereby the instrument manufacturer can be paid a fair percentage of the yield improvement in return for earlier instrument delivery to the process engineer, without the risk of taking a loss on the sale of the instrument. Such a financing agreement would benefit all parties involved.

## **Conclusions**

Many of the applications described for GaAs are applicable to silicon and other conductive materials as long as the sheet resistance of the processed layer is less than the substrate sheet resistance by a factor of at least 10. The instrument size can be varied to accommodate the size of the material being measured. Therefore, the yield improvements described are not limited just to wafers.



## Acknowledgements

Many thanks to the original authors of the excerpts used and the conferences and symposia where the papers were originally presented. We want to thank everyone who contributed to, typed and proofed this paper. We also want to acknowledge the hard work of the employees who have helped in the design and manufacturing of the instruments that have made the results shown possible. We appreciate the feedback from our customers of ideas for improvements.

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## About The Author

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