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Letter to the Editor

$In_{0.75}Ga_{0.25}As$ channel layers with record mobility exceeding 12,000 cm^2/Vs for use in high-κ dielectric NMOSFETs

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Abstract

$In_{0.75}Ga_{0.25}As$ channel layers with a record mobility exceeding 12,000 cm^2/Vs for use in high-κ dielectric NMOSFETs have been fabricated. The device structures which have been grown by molecular beam epitaxy on 3″ semi-insulating InP substrate comprise a 10 nm strained $In_{0.75}Ga_{0.25}As$ channel layer and a high-κ oxide based dielectric layer ($\kappa \cong 20$). Electron mobilities of 12,033 and 7,042 cm^2/Vs have been measured for sheet carrier concentrations n_s of 2.5×10^{12} and 6×10^{12} cm^{-2}, respectively.

Keywords: MOSFETs; Compound semiconductor; Charge carrier mobility; High-κ dielectrics

1. Introduction

SRC and SEMATECH recently announced plans to initiate a new ''Ultimate CMOS Device and Technology Transition Center'' related to extending CMOS beyond the 22-nm node of the current International Technology Roadmap for Semiconductors (ITRS). High priority has been assigned to III–V semiconductors as channel material driven by the need to enhance channel transport as well as to reduce power dissipation. Channel electron mobilities of 20,000 cm^2/Vs and higher appear to be useful for lowest power consumption. In the past, high-mobility III–V channel materials such as InSb and InAs were used in Schottky-gate quantum well transistors with measured electron mobilities exceeding 30,000 cm^2/Vs for a sheet carrier concentration n_s of 10^{12} cm^{-2} in InSb channels [1,2]. Electron mobilities of 19,000 cm^2/Vs were measured in InAs/AlSb quantum wells for a high n_s of 8×10^{12} cm^{-2} [3]. However, the reported Schottky gate devices operated in depletion (NMOSFET threshold voltage $V_{th} < 0$ V), an operational mode which is of minor interest. On the other hand, enhancement-mode NMOSFETs (threshold voltage $V_{th} > 0$ V) are of particular commercial interest based on their compatibility with present RF and silicon CMOS design approaches.

Recently, the first high-mobility enhancement-mode NMOSFETs using a III–V channel material have been manufactured [4]. The strained $In_{0.3}Ga_{0.7}As$ channel NMOSFETs grown on GaAs substrate operate in enhancement mode ($V_{th} > 0$ V) with electron mobilities of $\cong$4500 cm^2/Vs. A gate oxide technology with low interface state density [5,6] and a new, implant-free device concept [7] are fundamental prerequisites of the enhancement mode NMOSFETs in [4] and the device structures reported in this letter. Note that the implant-free device concept proposed in [7] and implemented in [4] does not utilize surface inversion to achieve enhancement mode and is therefore more suitable for high channel mobility. Further, enhance-

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ment mode operation is accomplished by using a high workfunction gate metal [4,7].

This letter reports on strained $In_{0.75}Ga_{0.25}As$ channel layers with even higher electron mobility exceeding 12,000 cm^2/Vs for use in high-κ dielectric NMOSFETs. The device layer structure is grown on InP substrate, includes a high-κ dielectric layer ($\kappa \cong 20$), and utilizes design criteria analogous to the layer structure of the enhancement mode NMOSFET on GaAs substrate reported in [4] and [8]. The reported transport properties are measured for ungated structures, i.e. under I_{on} conditions [4,7].

2. Experiment

$In_{0.75}Ga_{0.25}As$ channel layers for use in high-κ dielectric NMOSFETs have been grown on 3'' semi-insulating (SI) InP substrate by molecular beam epitaxy (MBE) using an ultra-high vacuum (UHV) dual chamber configuration. This configuration allows for the growth of the compound semiconductor epitaxial layers in one chamber and the deposition of the amorphous oxide film in a second chamber without exposing the semiconductor surface to atmosphere. Epitaxial layer growth is preceded by native InP oxide desorption in the presence of an As flux. Subsequent to epitaxial device layer growth, the wafer is cooled in the presence of an As flux and transferred to the oxide chamber via a UHV buffer transfer module. The wafer is then heated to a temperature between 400–450 °C, a Ga_2O_3 template layer is deposited and $(Gd_xGa_{1-x})_2O_3$ deposition is carried out to the target thickness. The resulting layer structure is shown in Fig. 1 and consists of a 0.5 μm undoped $In_{0.52}Al_{0.48}As$ buffer layer, a bottom Si δ-doping, a 4 nm undoped $In_{0.52}Al_{0.48}As$ layer, a 2 nm undoped $In_{0.53}Ga_{0.47}As$ layer, a 10 nm undoped and strained $In_{0.75}Ga_{0.25}As$ channel layer, a 2–4 nm undoped $In_{0.53}Ga_{0.47}As$ spacer layer, an optional top Si δ-doping, a 2–4 nm undoped $In_{0.52}Al_{0.48}As$ barrier layer, and an amorphous $Ga_2O_3/(Gd_xGa_{1-x})_2O_3$ ($x \cong 0.6$) dielectric stack with a Ga_2O_3 template layer thickness of 1 nm and a total nominal thickness of 20 nm [5]. Epitaxial layer composition has been determined in-situ using RHEED oscillations and ex situ using high resolution X-ray diffraction techniques; $(Gd_xGa_{1-x})_2O_3$ composition has been verified by Rutherford backscattering spectroscopy.

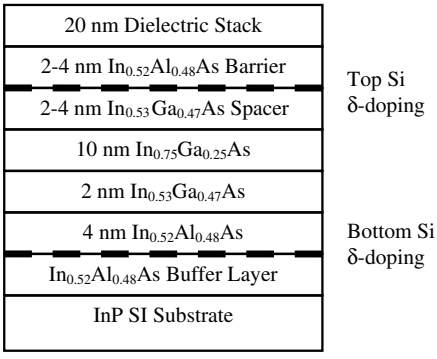

Fig. 1. InP based device layer structure with strained $In_{0.75}Ga_{0.25}As$ channel and high-κ dielectric. The δ-doped layers are indicated by dashed lines.

Electron transport properties including sheet resistivity ρ, sheet carrier concentration n_s, and electron mobility μ have been measured in the dark by a non-contact measurement method using the Lehighton Electronics Model 1610 Non-destructive Mobility Measurement System. Further details about the non-contact transport method can be found in [8]. The Hall technique bypasses issues such as channel resistance, gate leakage current, and contact resistance which need to be taken into account when using the drain current in the linear region of a FET to determine mobility [9]; issues which cannot be adequately addressed for a new technology in its infancy within the scope of this letter.

3. Results and discussion

Fig. 2 shows the measured channel electron mobility μ and sheet resistivity ρ as a function of the sheet carrier concentration n_s in the channel with the bottom/top silicon δ-doping concentrations (in units of $10^{12}\,cm^{-2}$) and the spacer layer thickness as parameters. The variations in sheet carrier concentration are accomplished by adjusting the bottom and/or top silicon δ-doping concentrations. For single-side doped (SSD) device structures, the bottom δ-doping concentration is varied in between 1.5–$3\times10^{12}\,cm^{-2}$ with the top δ-doping concentration being 0, while the top δ-doping concentration is also varied ($1.5–4.8\times10^{12}\,cm^{-2}$) for the double-side doped (DSD) device structure. The highest electron mobility of 12,033 cm^2/Vs is measured in a SSD device structure with n_s of $2.5\times10^{12}\,cm^{-2}$; the highest sheet carrier concentration $n_s = 6\times10^{12}\,cm^{-2}$ is obtained in a DSD device struc-

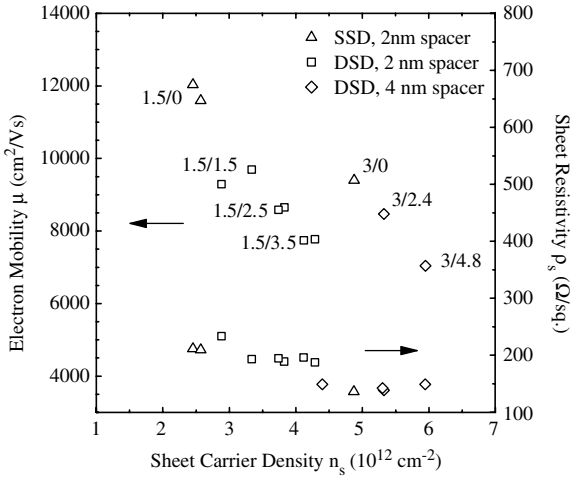

Fig. 2. Measured channel electron mobility μ and sheet resistivity ρ as a function of the sheet carrier concentration n_s in the channel with the bottom/top silicon δ-doping concentrations (in units of $10^{12}\,cm^{-2}$) and the spacer layer thickness as parameters. Data for both single-side doped (SSD, triangle) and double-side doped (DSD, square and diamond) device structures are shown.

ture with $\mu = 7{,}042\ \mathrm{cm}^2/\mathrm{Vs}$. As expected, mobilities in DSD device structures improve when the spacer layer thickness is increased from 2 nm (square) to 4 nm (diamond). The decrease in mobility with increasing n_s is attributed to remote ionized impurity scattering and population of the $In_{0.53}Ga_{0.47}As$ spacer layer. The sheet resistivity ρ ranges in between 233 and 136 Ω/sq. and is decreasing with increasing n_s.

In a further experiment, the gate dielectric layer was completely removed on one of the above reported device structures using wet chemical etching. The sheet resistivity increased from 136 to 3870 Ω/sq. indicating a dramatic degradation in sheet carrier concentration and/or mobility after gate oxide removal. Mobility and sheet carrier concentration were not separately determined after oxide removal.

4. Summary

Strained $In_{0.75}Ga_{0.25}As$ channel layers for use in high-κ dielectric NMOSFETs have been fabricated on InP substrate. The record electron mobilities of 12,033 and 7,042 $\mathrm{cm}^2/\mathrm{Vs}$ for n_s of 2.5×10^{12} and $6 \times 10^{12}\ \mathrm{cm}^{-2}$, respectively, exceed the previously reported [8] highest numbers for NMOSFETs by about a factor 2 and constitute yet another step towards MOSFET circuits designed for very low power operation. The increase in electron mobility is mainly attributed to the higher In mole fraction in the channel.

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