Application of IVS Overlay Measurement to Wafer Deformation Characterization Study

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Abstract

This work revealed one of the applications of overlay error measurement on investigation of GaAs wafer distortion during the normal high-temperature thermal process (above 800°C), using IVS overlay system. The results showed good correlation between the IVS overlay measurement and the temperature variation maps of the wafers obtained from temperature graduation experiments and electrical tests. The overlay error increased with increasing temperature.

INTRODUCTION

Overlay performance may be affected by various factors, such as the quality and location of the alignment marks, tool control and wafer distortion during the process. As part of an ongoing program of yield improvement, an investigation was conducted into distortion of 6" GaAs substrates, by evaluating registration data measured with an IVS120 overlay CD tool [1].

Overlay Yield Map analysis using the modeled data displays or predicts field yield across the entire wafer defined as error limit of misalignment quantified by a specification limit. This analysis provides information on overlay performance of the process.

Outer bar of the bar-in-bar feature for overlay performance measurement (registration) is pre-etched at PCM area located at the center of every field. Figure 1 shows a schematic drawing for the registration feature [1].

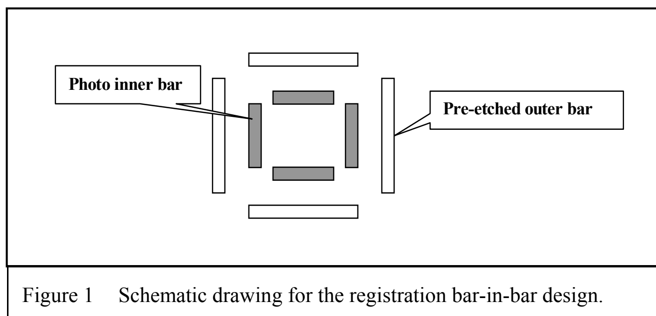

Figure 1 Schematic drawing for the registration bar-in-bar design.

EXPERIMENTAL

1) Wafer preparation: The experiment was designed to simulate the production processes as closely as possible. First, the alignment keys for stepper overlay alignment and bar in bar features for overlay registration measurement were etched into the GaAs test wafers. See Figure 1 for details of bar-in-bar features. Thus a photo layer was processed and registration was measured at every field across each wafer to set up a reference for the succeeding layer. The wafers then underwent the high temperature treatment, annealing. The wafers were oriented differently before being loaded into the RTA chamber. Various final temperatures and temperature ramp rates were used in these tests. As detached under the Result and Discussion section for details. Finally, the photo layer was applied on the wafers in order to obtain the overlay performance error at all the fields.

2) Measurements on IVS120 Optical Overlay CD System: All the wafers were measured for registration using IVS120 CD System, Schlumberger ATE. In total 126 fields were measured, symmetrically located across the wafer.

3) Split production lots under manufacturing conditions: Split production lots were processed using production quality wafers manufactured by different vendors and going through the entire process for the product.

RESULTS AND DISCUSSION

1) Parameters affecting wafer distortion -- temperature, ramp rate and wafer orientation[1,2]

Based on the experimental results, the wafer overlay is less affected by heat treatment (RTA) when placing the notch of a wafer in the cassette facing to the RTA chamber before it is loaded into the chamber. The process-introduced misalignment appears to be less when wafer notch was pre-aligned towards certain orientations in the RTA chamber.

The GaAs wafer can badly be distorted with increasing temperature. The maximum overall overlay error could be increased 0.15µm with a temperature change from 800°C ~

840°C. However, the error remained constant if temperature was varied in the range of 840~920°C as shown in Figure 2.

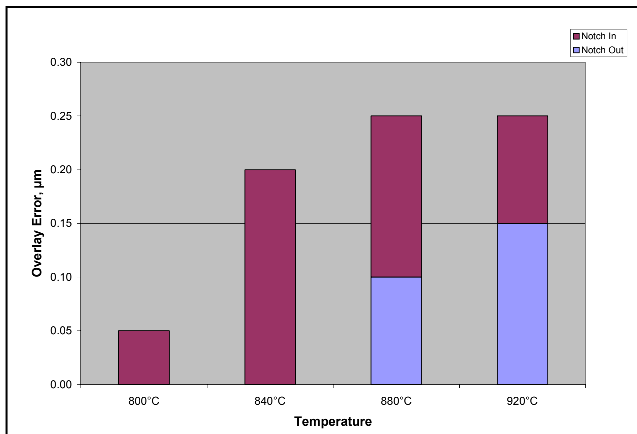

Figure 2 Temperature impact on overall overlay error

2) Effect of the substrate – GaAs material [1]

That the GaAs wafers manufactured by different vendors more or less undergo different processes is well known. A slight difference in the crystal growth process may result in unusual mechanical deformation of the wafers during high temperature thermal processing. The failures seen were due to leakage current in regions where the registration error became too great for the circuit to meet spec.

Two lots of the same material sensitive device were split using wafers supplied from different vendors. The wafer orientation for RTA was varied for both lots. The wafers were processed, as much as possible, under the same production conditions. The wafers of vendor A resulted in a lower total die sort yields especially at certain wafer orientations. The other observation in this experiment is that the wafers provided by the same vendor (vendor A) show higher variation in the same lot, which was as large as 20% in comparison to a 5% variation from vendor B. The lot average die sort yield of vendor A equaled 87% and vendor B 95%.

Figure 3 illustrates the die sort yield comparison on the wafers from three different materials (vendors), six lots randomly selected from each vendor. Among those lots, the yield loss was mainly from the low breakdown voltage between the gate and source or gate and drain at electrical test. The schematic drawing for the gate, drain and source illustrates the relationship among the parameters, in figure 4.

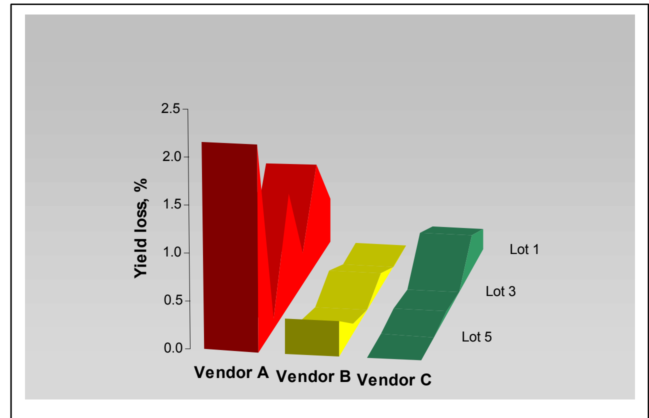

Figure 3 Comparison on die sort yield loss among different GaAs substrate.

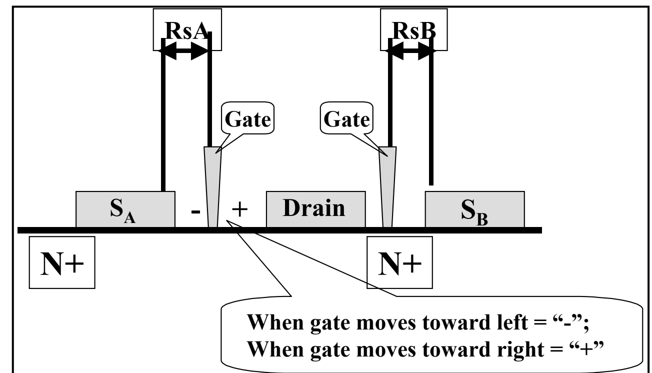

Figure 4 Schematic drawing for Gate, Drain and Source.

3) The correlation between IVS overlay error measurement and electrical test

As the box-in-box and gate test feature for monitoring gate-drain and gate-source breakdown voltage are located fairly close (3000um) to each other , a very good correlation was obtained between the gate test and registration measurement results. Illustrated in figure 5, a linear curve fitting describes the results from both test/measurement.

4) The correlation between IVS overlay error measurement and temperature sheet rho map

A good correlation observed between temperature sheet rho and the misalignment error measured on IVS. Figure 6 & 7 gives an example on the relationship. At the top corner, the sheet rho measured low, which represented higher temperature, while at the same region the misalignment yielded high.

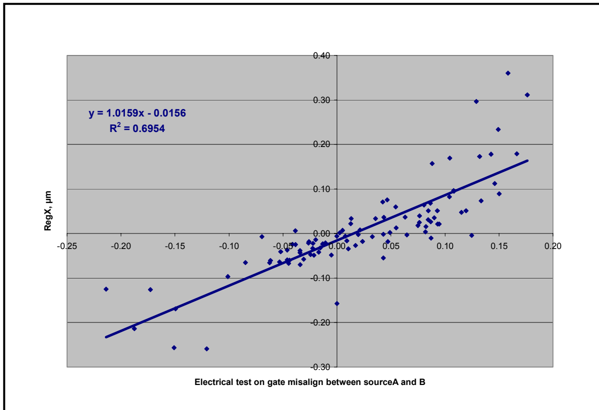

Figure 5 Correlation between electrical misalignment error test vs. IVS overlay measurement

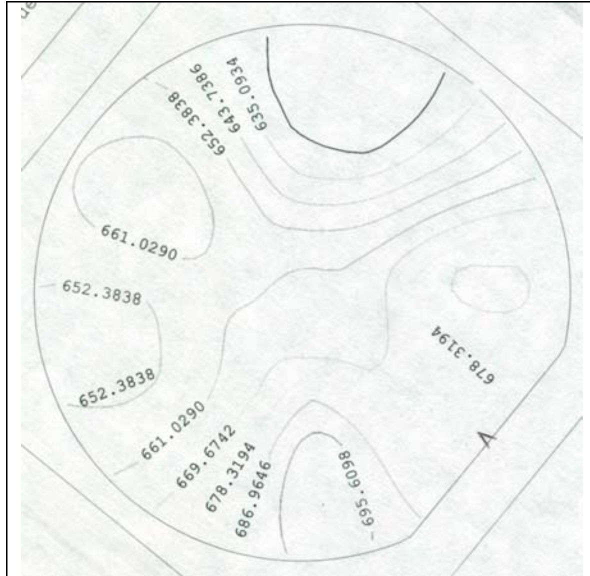

Figure 6 Example (880°C) of sheet rho maps of a wafer. Note low sheet rho is high temperature (lowest sheet rho in upper corner).

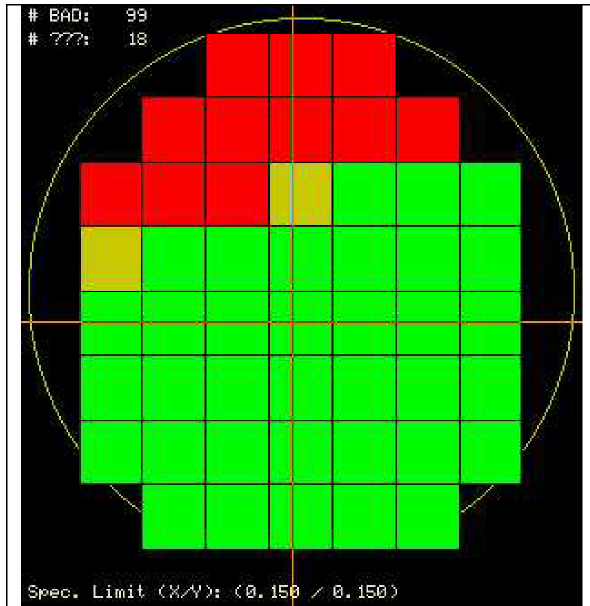

Figure 7 MONO-LITH analysis on registration error of IVS overlay measurement on the same wafer as shown in Figure 1. Higher temperature area with larger overlay error

CONCLUSIONS

The results in this work showed good correlation between the IVS overlay measurement and the temperature variation maps of the wafers obtained from temperature gradient experiments. Besides, the electrical tests yielded a good linear correlation with the IVS registration measurement when the test feature is located relativel7y close to the registration box-in-box.

ACKNOWLEDGEMENTS

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REFERENCES

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[2] Y. Liu and I. Black, *GaAs wafer overlay performance effected by annealing heat treatment: Part II*, SPIE (2002) - Metrology, Inspection, and Process Control for Microlithography XVI, pp. 616-623, March 2002.