Transition of SiC MESFET Technology from Discrete Transistors to High Performance MMIC Technology

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Keywords: SiC, MESFET, MMIC, HPSI, HTOL, GaN

Abstract

Significant progress has been made in the development of SiC MESFETs and MMIC power amplifiers manufactured on 3-inch high purity semi-insulating (HPSI) 4H-SiC substrates. MESFETs with a MTTF of over 200 hours when operated at a $T_{\rm J}$ =295 °C are presented. High power SiC MMIC amplifiers are shown with excellent yield and repeatability using a released foundry process. GaN HEMT operating life of over 500 hours at a $T_{\rm J}$ =160 °C is shown. Finally, GaN HEMTs with 30 W/mm RF output power density are reported.

INTRODUCTION

SiC MESFETs offer significant advantages for next generation commercial and military systems. Increased power density and higher operating voltage enable higher performance, lighter weight, and wider bandwidth systems. The transition to 3-inch HPSI 4H-SiC substrates (see Figure 1) and high uniformity SiC epitaxy in late 2002 has facilitated continued improvement in both SiC MESFET performance and intrinsic device reliability [1]. In addition to providing a lower cost platform, the larger diameter substrates have also accelerated the maturation of a stable 3-inch SiC MMIC process for which commercial foundry services were initiated in mid 2003. The ability to fabricate complex, high power SiC MMICs allows another degree of freedom for systems engineers in the development of next generation radar, EW, and communication systems.

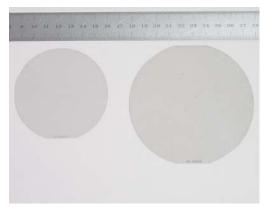


Figure 1: 3-inch and 100mm HPSI SiC substrates

SIC MESFET DEVICE PERFORMANCE

SiC MESFETs continue to mature in performance and manufacturing process stability. These devices now achieve a power density of approximately 4.0 W/mm and power added efficiencies greater than 50% on a regular basis. As an example, Figure 2 shows a 1.0 mm gate periphery MESFET operating at 50V producing 4.0 watts of output power at 66% drain efficiency (54% PAE) at 3.5 GHz.

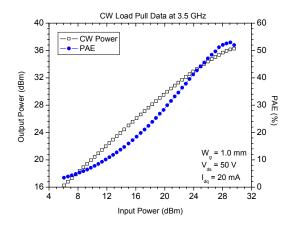


Figure 2: On-wafer CW load pull measurement of SiC MESFET with 4.0 W/mm and 66% drain efficiency.

One application for which there is increasing interest in the use of SiC MESFETs is in the area of wide band military communications. New U.S. DoD programs, such as JTRS, are pushing the limits for wide bandwidth, high efficiency amplifier performance using conventional technology. The higher output impedance of SiC MESFETs facilitates matching over much broader bandwidths than possible with silicon or GaAs transistors. As shown in Figure 3, over 10 dB of gain was achieved from 1 to 900 MHz with a standard (commercially available) 10 watt SiC packaged MESFET. No internal matching was required within the package to achieve this performance.

Swept Power and Gain for CRF-24010 in a Wideband Test Fixture

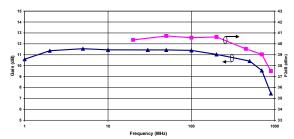


Figure 3: Measured broadband performance of a prototype circuit demonstrating >10 dB of gain from 1 to 900 MHz with no internal package matching.

SIC MESFET RELIABILITY

Reliability studies conducted on 10-watt SiC MESFETs fabricated on HPSI substrates demonstrate robust device characteristics. Figure 4 shows data from a DC accelerated life test on twenty 10-Watt SiC MESFETs operating at a T_J = 295°C. Every hour, the parts were cooled to a junction temperature of 175°C and the drain current was measured. After 210 hours, the average reduction in saturated drain current was approximately 10%. The corresponding reduction in saturated RF output power was 1dB for half the device population under test. This MTTF of 210 hours at T_J=295 °C is as good or better than that reported for GaAs devices even though the SiC devices were operated at a power density four times higher.

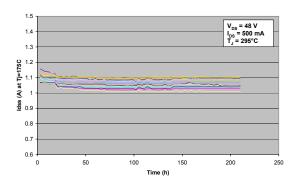


Figure 4: DC high temperature operating life (HTOL) data on twenty 10-Watt SiC MESFETs operating at T_J = 295°C showing minimal degradation after 210 hours. DC power dissipation was 4W/mm.

SiC MMIC FOUNDRY PROCESS

Given the rapid progress in the technical performance and reliability of SiC device technology, the focus during the last two years has shifted toward process stability, yield improvement, and higher levels of integration (i.e. SiC MMIC development) with the goal of becoming a high volume, low cost supplier of the technology. With that as the objective, a three-year program was initiated in July of 2002 for the conversion of our process to a 3-inch line. The cooperative program is supported, in part, with funding from the US Navy, the Missile Defense Agency, and the Department of Defense's Title III program. This program builds upon prior demonstrations of SiC MMIC capability in a 2-inch process. The program aims to enhance the producibility of SiC MMICs via yield improvements and will reduce the timeline for insertion into a variety of DoD applications. To date, the program has been very successful and the conversion to 3-inch substrates is now complete.

The rapid progress on this program has also allowed Cree to offer the first wide-bandgap semiconductor MMIC foundry service. Table 1 summarizes the typical performance of the unit cell transistor available from the foundry process.

Drain Voltage	50 V
Gate length	0.45 μm
P _{3dB} Power Density	4 W/mm
PAE at P _{3dB}	50%
Linear Gain at 3.5 GHz	12 dB

Table 1: Typical performance FET unit cell performance for the foundry process.

The MMIC process is very similar to existing GaAs MMIC processes in that it offers thinned substrates, thin-film resistors, high voltage MIM capacitors, spiral inductors, and through-wafer vias to accommodate FET source grounding and grounding for MMIC microstrip circuit elements. Un-thinned coplanar designs can also be fabricated. The process supports MMIC amplifier performance up to 6 GHz depending on bandwidth and gain requirements.

Figure 5 shows a DC yield map of a large, high power, SiC MMIC amplifier fabricated using the foundry process. The figure shows a threshold voltage (V_{th}) yield of 63% while 78% of the parts tested also satisfied the 100-volt drain-source breakdown voltage (V_{br}) requirement. These yield numbers are excellent for a large, high power MMIC power amplifier. Figure 6 shows an overlay of small signal gain for twenty-eight high power MMIC amplifiers fabricated on a 3-inch SiC substrate. The frequency and power information have been removed from the graph for classification reasons. It can be clearly seen, however, that the gain shape and part repeatability are indicative of a very uniform process. The two outlying gain curves were a result of physical damage to the parts during handling.

					-11	-10.6	-10.6	-10.6	-10.4	-10.4					
								-10.3		-10.1					
				40.0									40		
		-11.2	-11	-10.6	-10.5	-1U.4	-10.3	-10.8	-10	-9.9		-9.8	-10		
	-11.4	-11	-10.7	-10.6	-10.4		-10.3	-10.2	-10	-9.8	-9.8	-9.6			
			-10.6			-10.3	-10.2	-10.2	-10	-9.8		-9.4	-9.3	-9.6	
-11.6		-10.5	-10.5	-10.4	-10.3	-10.3	-10.2	-10.1	-10		-9.5	-9.3	-9.1	-9.2	
	-10.6	-10.3	-10.2	-10.2	-10.1	-10.1	-10.2	-9.8	-9.7	-9.5	-9.3	-9.1	-9	-8.9	
		-10.2	-10.1	-10.2		-9.8	-9.7	-9.6	-9.6		-9.3	-9.1	-8.9		
	-10.3	-10.1	-10	-9.9	-10	-9.7	-9.6	-9.4		-9.2	-9.2	-8.9	-8.7	-8.7	
-11.3	-10.5		-9.9	-9.8	-9.6	-9.6	-9.4	-9.3	-9.2	-9.1	-8.9	-8.7		-8.6	-9.1
		-10	-9.8	-9.6		-9.5	-9.2	-9.1	-9.1	-8.9	-8.7	-8.6	-8.6	-8.7	-9.4
			-9.7			-9.3	-9	-9	-9	-8.8		-8.5	-8.7	-8.9	
					-9.2	-9.1	-8.9	-8.9			-8.7	-8.5	-8.8		
				-9.5		-9	-8.9		-8.8			-8.9	-10		
					-9.5	-9.2	-9.1	.9	-9	-9.1					
							-10.3	-10.3	-10.9						

Figure 5: DC yield map for a large SiC MMIC power amplifier. Shaded areas are devices passing 100 V_{br} demonstrating a 78% yield. The V_{th} yield is 63% to a $\,$ 10V +/- 1.0V target.

Figure 7 shows an overlay of output power versus input power for a total of eighty-six (86) high power SiC MMIC power amplifiers across a six wafer foundry lot. As seen, the power response is extremely repeatable across all 86 amplifiers and all amplifiers that passed the small signal gain requirement also passed the output power goal. The data demonstrates that the process is extremely capable of producing large numbers of high performing MMIC power amplifiers with high yields.



Figure 6: Small signal gain of multiple high power MMICs on a single SiC wafer. Twenty-six out of twenty-eight parts met the RF gain requirement.

AlGaN/GaN HEMTs on HPSI SiC SUBSTRATES

In addition to SiC MMIC technology, considerable progress is also being made in the development of Gallium Nitride-on-SiC HEMT epitaxy and devices. Figure 8 shows a sheet rho uniformity map demonstrating a uniformity of 0.25% across a 3-inch SiC wafer. The best uniformity achieved to date is 0.22% with a median value of 1.2% observed on 630 3-inch SiC wafers across multiple epi runs.

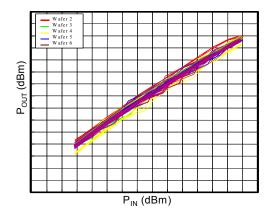


Figure 7: Pout vs. Pin for 86 high power SiC MMICs across six wafers. All MMICs that met small signal gain also passed output power requirements.

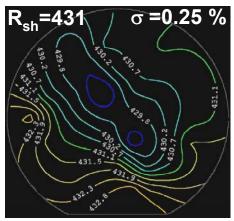


Figure 8: Sheet resistivity map for AlGaN/GaN HEMT epitaxy on 3-inch SiC showing excellent uniformity (0.25%).

The progress in GaN epitaxy has also led to a rapid improvement in both GaN device performance and reliability characteristics over the last 24 months. GaN power densities greater than 10 W/mm have been reported for HEMTs using new epitaxial barrier layers and doped buffers. These new epi structures have also been combined with device field-plate structures to produce record power density and efficiency. Figure 9 shows a power plot of an advanced GaN HEMT incorporating an AlN barrier with an Fe-doped buffer to produce over 30 W/mm RF power density with an associated power added efficiency of 55%. These devices were operated at a drain voltage of 120 volts which is well in excess of the typical 30-40 volt operation seen in the industry.

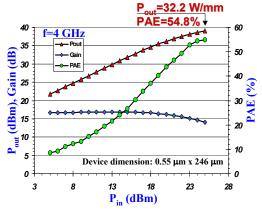


Figure 9: High performance GaN HEMT incorporating an AlN barrier, Fe-doped buffer, and device field-plate technology.

Steady improvements are also being made with regard to GaN HEMT reliability. Although considerable work remains, Figure 10 shows a plot of relative device output power and absolute drain current versus time for our best devices. As seen, there is no measurable change in either parameter over 500 hours of device operation at a junction temperature of 160°C. This part was biased at a drain voltage of 28 volts and held at 2dB RF gain compression at a frequency of 4 GHz. The room temperature P_{3dB} RF output power density and PAE were 3.4W/mm and 66% respectively both before and after the applied stress.

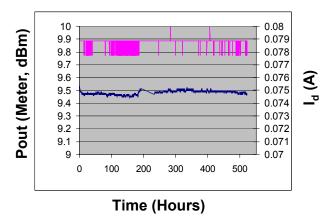


Figure 10: In-situ P_{out} and I_{DS} data for a GaN HEMT at: V_{DS} = 28 V, I_{DS} = 79 mA, T_J = 160°C, and f_o =4 GHz. The part was held at 2 dB RF gain compression.

CONCLUSIONS

SiC MESFETs have now been transitioned to 3-inch production capability and are commercially available. SiC device yields, reliability, and MMIC processing are now sufficiently mature to support large, complex SiC MMICs. These power amplifier circuits are now available to systems designers via SiC MMIC foundry services. GaN HEMTs are also maturing both in performance and reliability characteristics.

ACKNOWLEDGEMENTS

The work discussed in this paper has been supported in part by contracts (N00014-C-02-0306) and (N00014-C-02-0250). Both contracts are monitored by Dr. Harry Dietrich through the Office of Naval Research.

REFERENCES

[1] J.W. Milligan, S.T. Allen, J.J. Sumakeris, A.R. Powell, J.R. Jenny, and J.W. Palmour, "Transition of High Power SiC MESFETs from 2-inch to 3-inch Production for Improved Cost and Producibility", GaAs MANTECH Conference Digest of Papers, Scottsdale Az. (2003).

ACRONYMS

SiC: Silicon Carbide

HPSI: High Purity Semi-insulating HTOL: High Temperature Operating Life

MESFET: Metal Semiconductor Field Effect Transistor

GaN: Gallium Nitride

HEMT: High Electron Mobility Transistor

MTTF: Mean Time to Failure JTRS: Joint Tactical Radio System