High Mobility NMOSFET Structure With High-κ Dielectric

Matthias Passlack, *Senior Member, IEEE*, Ravi Droopad, *Member, IEEE*, Karthik Rajagopalan, *Member, IEEE*, Jonathan Abrokwah, *Senior Member, IEEE*, Rich Gregory, and Danh Nguyen

***Abstract*—High-κ NMOSFET structures designed for enhancement mode operation have been fabricated with mobilities exceeding 6000 cm^2/Vs. The NMOSFET structures which have been grown by molecular beam epitaxy on 3-in semi-insulating GaAs substrate comprise a 10 nm strained InGaAs channel layer and a high-κ dielectric layer ($\kappa \cong 20$). Electron mobilities of > 6000 and 3822 cm^2/Vs have been measured for sheet carrier concentrations n_s of 2–3 $\times 10^{12}$ and $\cong 5.85 \times 10^{12}$ cm^{-2}, respectively. Sheet resistivities as low as 280 Ω/sq. have been obtained.**

***Index Terms*—Charge carrier mobility, high-κ dielectrics, MOSFETs.**

I. Introduction

CHARGE carrier mobility continues to be a key parameter for MOSFET performance beyond the 90-nm technology node of the International Technology Roadmap for Semiconductors (ITRS). Typical electron mobilities in Si MOSFETs with SiO_2 gate dielectric are around 500–600 cm^2/Vs for inversion charge densities $\cong 2-3 \times 10^{12}$ cm^{-2} [1]. Mobility enhancement factors between 1.6 and 2 were measured using layers of strained SiGe or Ge, respectively [2]–[4]. However, the use of high-κ dielectrics such as HfO_2 reduces mobility; typical peak electron mobilities for Si bulk MOSFETs with HfO_2 gate dielectric are 200 cm^2/Vs [1], [5]. A future alternative to Si bulk and Si-based strained layer MOSFETs are layer structures based on III-V compound semiconductors [6], [7]. For the first time, the latest edition of the ITRS roadmap includes serious references to compound semiconductor based transistors as a "nonclassical" CMOS solution to continue long term scaling according to Moore's Law. Further, a number of RF applications, in particular in the wireless and mobile product space, will benefit from performance enhancements potentially provided by III-V MOSFETs. This letter reports on electron mobilities as high as 6,155 cm^2/Vs in GaAs enhancement mode NMOSFET structures employing a high-κ dielectric ($\kappa \cong 20$) and a strained InGaAs channel layer with a thickness of 10 nm.

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M. Passlack, R. Droopad, K. Rajagopalan, J. Abrokwah, and R. Gregory are with Freescale Semiconductor Inc., Tempe, AZ 85284 USA (e-mail: m.passlack@freescale.com).

D. Nguyen is with Lehighton Electronics, Lehighton, PA 18235 USA.

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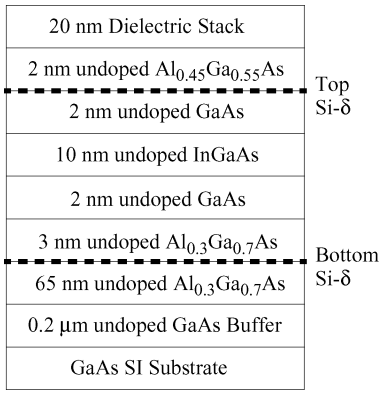

Fig. 1. NMOSFET layer structure. The δ-dopings are indicated by dashed lines.

II. Experiment

NMOSFET wafers have been grown on 3-in semi-insulating (SI) GaAs substrate by molecular-beam epitaxy (MBE) using an ultrahigh vacuum (UHV) dual chamber configuration manufactured by DCA. The GaAs epitaxial layer structure is grown in the first chamber (III-V chamber) and the gate oxide in the second chamber (oxide chamber) wherein the wafer is transferred from the first to the second chamber via a UHV transfer module. The layer structure is shown in Fig. 1 and consists of a 0.2-μm undoped GaAs buffer layer, a 65-nm undoped $Al_{0.3}Ga_{0.7}As$ layer, a bottom Si δ-doping, an undoped bottom spacer layer including 3 nm of $Al_{0.3}$ $Ga_{0.7}As$ and 2 nm of GaAs, a 10-nm undoped $In_yGa_{1-y}As$ ($0.27 \leq y \leq 0.31$) channel layer, a 2-nm undoped GaAs top spacer layer, a top Si δ-doping, a 2-nm undoped $Al_{0.45}Ga_{0.55}As$ barrier layer, and an amorphous $Ga_2O_3/(Gd_xGa_{1-x})_2$ O_3 ($x \cong 0.6$) dielectric stack with a Ga_2O_3 template layer thickness of $\cong 1$ nm and a total nominal thickness of 20 nm. The In mole fraction of the InGaAs channel layer has been measured by X-ray diffraction. The fabrication of the NMOSFET structure further includes a post- deposition annealing step which is performed subsequent to MBE growth. Typical electrical parameters of the dielectric stack such as a midgap interface state density $D_{\rm it}$ ($\cong 2 \times 10^{11}$ cm^{-2}eV^{-1}) on GaAs and a dielectric constant κ of 20 were reported elsewhere [8], [9]. The NMOSFET layer structure is designed for enhancement mode operation, i.e., an NMOSFET threshold voltage $V_{\rm th} > 0$. Details about the basic concept of implant-free, high mobility MOSFETs can be found in [10], [11]. For reference purposes, a standard pseudomorphic high electron mobility transistor (PHEMT) structure in which

TABLE I
TRANSPORT DATA OF GaAs NMOSFET AND PHEMT STRUCTURES

Structure			Transport Data					
Type	δ-Doping (10^{12} cm^{-2})		Electron Mobility (cm^2/Vs)		Sheet Carrier Density n_s (10^{12} cm^{-2})		Sheet Resistivity ρ_s (Ω/sq.)	
	Bottom	Top	Mean	σ	Mean	σ	Mean	σ
MOSFET	6	0	6155	120.4	2.42	0.05	422.6	17.9
	6	1	6012	26.1	2.85	0.02	367.1	2.1
	6	2	5303	24.9	3.61	0.05	328.5	4.7
	6	4	4447	3.6	5.03	0.01	280.0	0.5
	6	6	3822	10.7	5.85	0.07	280.3	4.3
PHEMT	6	0	5726	32.7	1.57	0.03	696.2	7.9

the gate dielectric is replaced by a 30-nm GaAs cap layer has also been grown.

NMOSFET electron transport properties have been measured by a noncontact measurement method using the Lehighton Electronics Model 1610 Nondestructive Mobility Measurement System. This system uses a low-power microwave source operating at 10 GHz, coupled to a waveguide network, to direct the power to the surface of the wafer under test. The waveguide network allows detection and measurement of both the TE10 and TE11 modes of propagation. The normal TE10 incident wave is used to generate two types of reflected waves returned from the sample under test. The first wave, the reflected power, is in the same mode (or polarization) as that of the incident wave. The power from this reflected wave is detected, measured, and used to calculate the sample's sheet resistivity ρ_s based on the overall impedance of the waveguide system. The second wave, the TE11 mode, is caused by the "Hall Effect" of the sample under the influence of a magnetic field. The normal TE10 incident wave is rotated 90 degrees by this effect. The system detects and measures the Hall power, and uses this to calculate the remaining transport properties of mobility μ and sheet carrier density n_s. An internal study conducted at Lehighton comparing transport data of PHEMT and HBT devices on various material systems has shown the noncontact transport data to be within 10% of standard dc Hall measurements. All Hall mobility measurements were done in the dark at room temperature (RT). The difference between Hall mobilities and effective channel mobilities determined by the split C–V method is typically less than 10% [1], [12].

III. RESULTS AND DISCUSSION

Measured transport data for GaAs based NMOSFET structures with different bottom and top δ-doping concentrations are summarized in Table I. The reported transport properties are measured for ungated NMOSFET structures under nearly flatband condition. Note that for an implant-free NMOSFET device, flatband is observed at the source side of the gate under $I_{\rm on}$ conditions. Enhancement mode operation (threshold voltage $V_{\rm th} > 0$) is accomplished by using a high workfunction gate metal [11]. For comparison purposes, transport data for a reference PHEMT structure are given with a bottom and top δ-doping of 6×10^{12} cm^{-2} and 0, respectively. The sheet carrier density of the corresponding NMOSFET structure

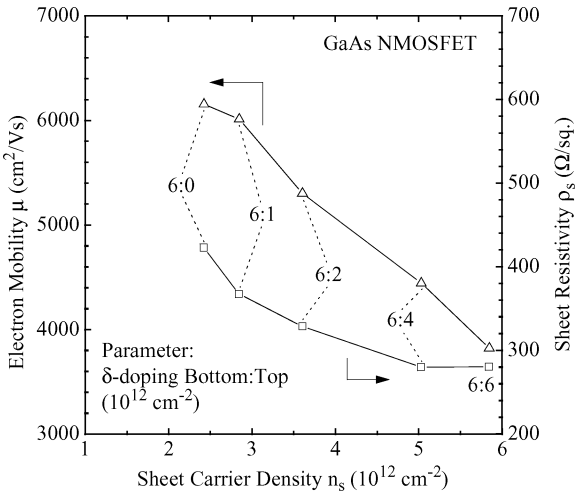

Fig. 2. Mobility (triangles) and sheet resistivity (squares) of NMOSFET structure as a function of the sheet carrier density in the channel with the concentrations of the bottom and top δ-dopings in units of 10^{12} cm^{-2} (bottom:top) as parameter.

(2.42×10^{12} cm^{-2}) is 8.5×10^{11} cm^{-2} higher compared to the PHEMT structure (1.57×10^{12} cm^{-2}). Calculations using a Poisson's solver show that the trapped surface charge density on the PHEMT structure under the assumption of surface Fermi level pinning at 0.7–0.8 V below the GaAs conduction band edge is 1.0–1.2×10^{12} cm^{-2}. Thus, only 1.5–3.5×10^{11} cm^{-2} of trapped charge remains in the NMOSFET structure. This trapped charge could be either located on the oxide surface or the oxide/semiconductor interface.

Fig. 2 shows the measured electron mobility (triangles) and sheet resistivity (squares) as a function of the sheet carrier density in the channel. The variations in sheet carrier density are accomplished by adjusting the δ-doping concentration, in particular the concentration of the top δ- doping. Typical electron mobilities exceeding 6,000 cm^2/Vs are measured for $n_s \cong 2 - 3 \times 10^{12}$ cm^{-2}. These mobilities are higher by a factor of $\cong 12$ and > 30 when compared to SiO_2 and high-κ dielectric Si based NMOSFETs, respectively. Electron mobilities for $n_s \cong 6 \times 10^{12}$ cm^{-2} are still approaching 4,000 cm^2/Vs. Sheet resistivities as low as 280 Ω/sq are measured for NMOSFET structures with higher sheet carrier density. This is a distinct advantage over ion-implanted GaAs technologies where sheet resistivity below 500 Ω/sq is difficult to obtain within the thermal budget of the technology ($\cong$ 700 °C).

Note that the $Al_{0.45}Ga_{0.55}As$ barrier layer serves a number of purposes which include widening of the semiconductor surface bandgap [10] and alleviating mobility degradation caused by interface and oxide traps as well as oxide soft-polar optical phonons. Widening of the surface bandgap is in particularly important in high mobility material systems because the effective density of states in the conduction band is considerably lower compared to Si (e.g., $N_c = 4.7 \times 10^{17}$ and 2.8×10^{19} cm^{-3} for GaAs and Si, respectively, [13]) and interface state densities typically rise toward the conduction band edge. The effect of further scaling of $Al_{0.45}Ga_{0.55}As$ barrier layer thickness on mobility has not been investigated in this study and no further scaling of layer thicknesses has been performed.

IV. Summary

Electron mobility in GaAs-based enhancement mode NMOSFET structures has been studied. Typical electron mobilities exceeding 6000 cm^2/Vs are measured for $n_s \cong 2 - 3 \times 10^{12}$ cm^{-2}. These mobilities are higher by a factor of 12 and > 30 when compared to SiO_2 and high-κ dielectric Si based NMOSFETs, respectively. For a sheet carrier concentration $n_s \cong 6 \times 10^{12}$ cm^{-2}, a mobility of 3822 cm^2/Vs has been obtained.

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