Top-Gated Epitaxial Graphene FETs on Si-Face SiC Wafers With a Peak Transconductance of 600 mS/mm


Abstract—In this letter, we present state-of-the-art performance of top-gated graphene n-FETs and p-FETs fabricated with epitaxial graphene layers grown on Si-face 6H-SiC substrates on 50-mm wafers. The current–voltage characteristics of these devices show excellent saturation with ON-state current densities \(I_{\text{on}}\) of 0.59 A/mm at \(V_{\text{ds}} = 1\) V and 1.65 A/mm at \(V_{\text{ds}} = 3\) V. On-set current-to-effective current ratios of 12 and 19 were measured at \(V_{\text{gs}} = 1\) and 0.5 V, respectively. A peak extrinsic \(g_m\) as high as 600 mS/mm was measured at \(V_{\text{ds}} = 3.05\) V, with a gate length of 2.94 μm. The field-effect mobility versus effective electric field \(E_{\text{eff}}\) was measured for the first time in epitaxial graphene FETs, where record field-effect mobilities of 6000 cm²/V·s for electrons and 3200 cm²/V·s for holes were obtained at \(E_{\text{eff}} \sim 0.27\) MV/cm.

Index Terms—Field-effect mobility, graphene, n-FET, p-FET, Si MOSFET, transistor.

Graphene, which consists of one or a few atomic layers of 2-D carbon sheets, has generated a lot of interest in the research community [1]. The intrinsic saturation velocity \(V_{\text{sat}}\) of graphene itself is expected to be at least two times faster [2] than that of lattice-matched InP HEMTs, the current material of choice for high-speed RF applications.

Epitaxial graphene FETs [3]–[7] on the wafer scale are in the early stages of development, although several key device parameters have been demonstrated. For example, epitaxial graphene RF FETs [7] have been demonstrated in a top-gated layout with the highest ever ON-state current density of 3 A/mm. In addition, the extrinsic speed performance \(f_1/f_{\text{max}}\) of 5 GHz/14 GHz is reported with a 2-μm gate length. On the other hand, the current–voltage characteristics are quasi-linear and poor voltage gain \(g_m\) was measured for the first time in epitaxial graphene FETs [7] with a peak extrinsic \(g_m\) as high as 600 mS/mm at \(V_{\text{ds}} = 3.05\) V, with a gate length of 2.94 μm. The field-effect mobility versus effective electric field \(E_{\text{eff}}\) was measured for the first time in epitaxial graphene FETs, where record field-effect mobilities of 6000 cm²/V·s for electrons and 3200 cm²/V·s for holes were obtained at \(E_{\text{eff}} \sim 0.27\) MV/cm.

In this letter, we present top-gated graphene n-FETs and p-FETs from epitaxial graphene layers, where excellent \(I-V\) saturation behaviors were observed for the first time in epitaxial graphene FETs with a peak record extrinsic transconductance of 600 mS/mm. Moreover, the effective mobility and field-effect mobility versus \(E_{\text{eff}}\) were characterized and compared with Hall mobility. The epitaxial graphene layers were grown on Si-face 6H-SiC substrates on 50-mm wafers via Si sublimation [9]. The sheet electron carrier density of the epitaxial graphene layer was typically \(8.8 \times 10^{12}\) cm⁻² at room temperature and had an electron mobility of \(\sim 192\) cm²/V·s, characterized by noncontact Hall Lehighton 1600. The number of epitaxial graphene layers \(n_{\text{GL}}\) was found to be one layer on the SiC terraces and two layers on the step edges over the entire 50-mm wafer as characterized by Raman analysis and transmission electron microscopy analysis.

Graphene FETs were fabricated with Ti/Pt/Au source and drain metal deposition and lift-off process. The nonalloyed ohmic metal yielded the contact resistivity of \(10^{-6} - 10^{-7} \ \Omega \cdot \text{cm}^2\) [7]. The metal gates were processed with Ti/Pt/Au metal deposition and lift-off process on top of a 35-nm-thick SiO₂ gate dielectric layer deposited by electron beam evaporation. The gate leakage current was in the range of approximately nanoamperes per square micrometer or less (see Fig. 3), which is negligible in the device characterization presented here.

Fig. 1(a) and (b) shows the graphene FET processed in a layout, where the gate metal is aligned with respect to the ohmic metals in an underlap layout with a gate-to-source/drain separation of \(< 100\) nm to minimize the access resistance over a source–drain spacing \(L_{\text{sd}}\) of 3 μm. The source access resistance was \(< 0.2 \ \Omega \cdot \text{mm}\) via the standard end-point measurements on transfer length method structures. A graphene channel width of 4 μm was defined by O₂ plasma etching.
Fig. 1. (a) Schematic of the top-gated graphene FET. (b) SEM photograph of 2f × 4 μm graphene FET. (c) Measured common-source current–voltage characteristics of 1f × 4 μm graphene FET.

Fig. 1(c) shows measured room-temperature common-source current–voltage characteristics of a two-gatefinger and 4-μm-wide n-channel graphene FET (denoted as 2f × 4 μm), in which excellent drain current saturation was observed. The source-to-drain voltage \( V_{\text{ds}} \) was swept up to 3 V, where the gate-to-source \( (V_{\text{gs}}) \) voltage was stepped from 3 V (top curve) in steps of −0.5 V. At \( V_{\text{ds}} = 1 \) V, the on-state current at \( V_{\text{gs}} = 3 \) V was 0.59 A/mm. The off-state current was 0.047 A/mm at \( V_{\text{gs}} = 0 \) V. The p-channel behavior was observed with threshold voltages \( (V_T) \) of −1.5 to −1.35 V, where \( V_T \) was set to be a Dirac point for an extraction of the effective mobility for graphene FETs.

Effective mobility \( \mu_{\text{eff}} \) was extracted using the following formula: \( \mu_{\text{eff}} = (L/W) \cdot \frac{I_{\text{ds}}}{|C_{\text{ox}} \cdot (V_{\text{gs}} - V_T) \cdot V_{\text{ds}}|} \) [10]. In the case of a finite charge density \( Q_{\text{Dirac}} \) at Dirac point, \( \mu_{\text{eff}} \) can be corrected accordingly.\(^1\) \( C_{\text{ox}} \) is the gate oxide capacitance, and \( \varepsilon_0 \cdot \varepsilon_{\text{ox}} / t_{\text{ox}} \) where \( \varepsilon_0 \) and \( \varepsilon_{\text{ox}} \) is permittivity of the free space and gate oxide layer, respectively. The gate oxide capacitance is measured using a metal–oxide–metal (MOM) capacitor array with OPEN and SHORT calibration standards. The geometric scaling of the MOM capacitors is verified to eliminate fringe capacitances. The geometric oxide capacitances were measured to be 1 or 1.7 \( \text{fF}/\mu\text{m}^2 \) from two different wafers. The dielectric constant of the deposited \( \text{SiO}_2 \) films was determined

\( ^1 \text{In graphene, the effective mobility can be defined as } \mu_{\text{eff}} = (L/W) \cdot \frac{I_{\text{ds}}}{|C_{\text{ox}} \cdot (V_{\text{gs}} - V_T) + Q_{\text{Dirac}}| \cdot V_{\text{ds}}|}. \) This could lead to about 10% correction in \( \mu_{\text{eff}} \), but not in \( \mu_{\text{FE}} \), compared to the values in the main text.
to be 3.9, which is close to that of SiO2. The field-effect mobility $\mu_{FE}$ defined by $\mu_{FE} = (I/W) \cdot g_{m}/(C_{ox} \cdot V_{ds})$ [10] was obtained from the transconductance ($g_{m}$) at $V_{ds} = 50$ mV. Therefore, there is no ambiguity in $\mu_{FE}$ associated with $V_{T}$, unlike the case of $\mu_{eff}$. The effective electric field is estimated using $E_{eff} = Q_{Gr}/(\xi_0 \cdot C_{ox})$, where $Q_{Gr}$ is the total charge in the graphene channel.

Fig. 4 shows the extracted $\mu_{eff}$ and $\mu_{FE}$ of graphene n-FETs versus the effective electric field $E_{eff}$. For comparison, the universal and field-effect mobilities of Si n-MOSFETs [11] and strained Si n-MOSFETs on SiGe-on-oxide [12] are shown. While both $\mu_{eff}$ and $\mu_{FE}$ of the graphene n-FETs depend on $E_{eff}$, both values were higher than 1000 cm$^2$/V·s over a wide range of effective electric field up to 1.6 MV/cm. The peak field-effect mobility values ranged from 3200 to 6000 cm$^2$/V·s depending on the devices shown in Fig. 3. A record field-effect mobility of 6000 cm$^2$/V·s was obtained at an effective electric field of 0.27 MV/cm from the device (□) shown in Fig. 3. To compare with the measured Hall mobility, which was measured at high carrier concentrations, both $\mu_{eff}$ and $\mu_{FE}$ curves versus $E_{eff}$ were extrapolated using $\mu_{eff} = 6806 \times E^{-0.36}E_{eff}$ for $C_{ox}$ of 1 fF/μm$^2$ and $\mu_{eff} = 6111 \times E^{-0.44}E_{eff}$ for $C_{ox}$ of 1.7 fF/μm$^2$. At the Hall carrier density of $(9-10) \times 10^{12}$/cm$^2$, the $\mu_{eff}$ values were extrapolated to be $1120$ cm$^2$/V·s for $C_{ox}$ of 1 fF/μm$^2$ and $670$ cm$^2$/V·s for $C_{ox}$ of 1.7 fF/μm$^2$. The extrapolated effective mobility values were close to the measured Hall mobility. On the other hand, the $\mu_{FE}$ was extrapolated to be $\sim 50$ cm$^2$/V·s at the Hall carrier density of $(9-10) \times 10^{12}$/cm$^2$. This is much lower than the measured Hall mobility of $\sim 1192$ cm$^2$/V·s. The measured field-effect mobilities of graphene n-FETs were at least seven times higher than that of ITRS Si n-MOSFETs and $\sim 80$ times higher than that of ultra-thin-body SOI n-MOSFETs. The peak field-effect mobility of graphene p-FETs was also determined to be 3200 cm$^2$/V·s at an effective electric field of 0.2 MV/cm.

While more studies are needed for quantitative analysis, the observed excellent $I$–$V$ saturation, high $I_{on}/I_{off}$ ratio, and high transconductance may be attributed to several factors, including the low source access resistance of $< 0.2 \Omega \cdot$ mm and the low trapped charge density. The capacitance–voltage measurement of the top-gate metal–SiO$_2$–graphene diodes was carried out, and the trapped charge density of the SiO$_2$ layer was estimated to be $\sim 2 \times 10^{11}$/cm$^2$, which improves the graphene channel mobility and, consequently, $g_{m}$. The improvement of the $I_{on}/I_{off}$ ratio may be due to a reduction in charge inhomogeneity near the Dirac point or a formation of a pinch-off region in a zero-bandgap graphene film [13]. We note that the possibility of a small bandgap associated with strained epitaxial graphene film is not excluded. We also note that the peak extrinsic $g_{m}$ of 600 mS/mm per unit gate capacitance of 1 fF/μm$^2$ yields a calculated gate delay of 2 ps/μm.

**REFERENCES**