Top-Gated Epitaxial Graphene FETs on Si-Face SiC Wafers With a Peak Transconductance of 600 mS/mm

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***Abstract*—In this letter, we present state-of-the-art performance of top-gated graphene n-FETs and p-FETs fabricated with epitaxial graphene layers grown on Si-face 6H-SiC substrates on 50-mm wafers. The current–voltage characteristics of these devices show excellent saturation with ON-state current densities ($I_{\rm on}$) of 0.59 A/mm at $V_{\rm ds} = 1$ V and 1.65 A/mm at $V_{\rm ds} = 3$ V. $I_{\rm on}/I_{\rm off}$ ratios of 12 and 19 were measured at $V_{\rm ds} = 1$ and 0.5 V, respectively. A peak extrinsic g_m as high as 600 mS/mm was measured at $V_{\rm ds} = 3.05$ V, with a gate length of 2.94 μm. The field-effect mobility versus effective electric field ($E_{\rm eff}$) was measured for the first time in epitaxial graphene FETs, where record field-effect mobilities of 6000 cm^2/V · s for electrons and 3200 cm^2/V · s for holes were obtained at $E_{\rm eff} \sim 0.27$ MV/cm.**

***Index Terms*—Field-effect mobility, graphene, n-FET, p-FET, Si MOSFET, transistor.**

GRAPHENE, which consists of one or a few atomic layers of 2-D carbon sheets, has generated a lot of interest in the research community [1]. The intrinsic saturation velocity ($V_{\rm sat}$) of graphene itself is expected to be at least two times faster [2] than that of lattice-matched InP HEMTs, the current material of choice for high-speed RF applications.

Epitaxial graphene FETs [3]–[7] on the wafer scale are in the early stages of development, although several key device parameters have been demonstrated. For example, epitaxial graphene RF FETs [7] have been demonstrated in a top-gated layout with the highest ever ON-state current density of 3 A/mm. In addition, the extrinsic speed performance $f_t/f_{\rm max}$ of 5 GHz/14 GHz is reported with a 2-μm gate length. On the other hand, the current–voltage characteristics are quasi-linear with weak saturation behaviors, yielding low transconductance (g_m) per capacitance (i.e., $<$ 140 mS/mm at 3.4 fF/μm^2) and poor voltage gain ($g_m/G_{\rm ds}$). In addition, the $I_{\rm on}/I_{\rm off}$ ratio was $\sim$4 with a field-effect mobility below 200 cm^2/V · s. While graphene field-effect mobility as high as 5400 cm^2/V · s for electron has been demonstrated [5], it was achieved using six to seven layers of epitaxial graphene on C-face SiC substrates, resulting in an $I_{\rm on}/I_{\rm off}$ ratio of < 2. In the case of graphene FETs fabricated on the Si-face of SiC substrates, field-effect mobility has been limited to below 1200 cm^2/V · s, but with an improved $I_{\rm on}/I_{\rm off}$ ratio of $\sim$10 [6]. The graphene effective mobility versus effective vertical electric field ($E_{\rm eff}$) was reported using top-gated exfoliated graphene FETs on SiO_2 substrates [8]. The exfoliated graphene top-gated FETs have shown an effective mobility below 3000 cm^2/V · s at $E_{\rm eff} < 0.1$ MV/cm, significantly less than $\sim$10 000 cm^2/V · s achieved from the back-gated graphene FETs.

In this letter, we present top-gated graphene n-FETs and p-FETs from epitaxial graphene layers, where *excellent I–V saturation behaviors were observed for the first time in epitaxial graphene FETs* with a record peak extrinsic transconductance of 600 mS/mm. Moreover, the effective mobility and field-effect mobility versus $E_{\rm eff}$ were characterized and compared with Hall mobility. The epitaxial graphene layers were grown on Si-face 6H-SiC substrates on 50-mm wafers via Si sublimation [9]. The sheet electron carrier density of the epitaxial graphene layer was typically 8.8×10^{12} cm^{-2} at room temperature and had an electron mobility of $\sim$1192 cm^2/V · s, characterized by noncontact Hall Lehighton 1600. The number of epitaxial graphene layers ($n_{\rm GL}$) was found to be one layer on the SiC terraces and two layers on the step edges over the entire 50-mm wafer as characterized by Raman analysis and transmission electron microscopy analysis.

Graphene FETs were fabricated with Ti/Pt/Au source and drain metal deposition and lift-off process. The nonalloyed ohmic metal yielded the contact resistivity of 10^{-6}–10^{-7} $\Omega \cdot$ cm^2 [7]. The metal gates were processed with Ti/Pt/Au metal deposition and lift-off process on top of a 35-nm-thick SiO_2 gate dielectric layer deposited by electron beam evaporation. The gate leakage current was in the range of approximately nanoamperes per square micrometer or less (see Fig. 3), which is negligible in the device characterization presented here.

Fig. 1(a) and (b) shows the graphene FET processed in a layout, where the gate metal is aligned with respect to the ohmic metals in an underlap layout with a gate-to-source/drain separation of $<$100 nm to minimize the access resistance over a source–drain spacing ($L_{\rm sd}$) of 3 μm. The source access resistance was < 0.2 $\Omega \cdot$ mm via the standard end-point measurements on transfer length method structures. A graphene channel width of 4 μm was defined by O_2 plasma etching.

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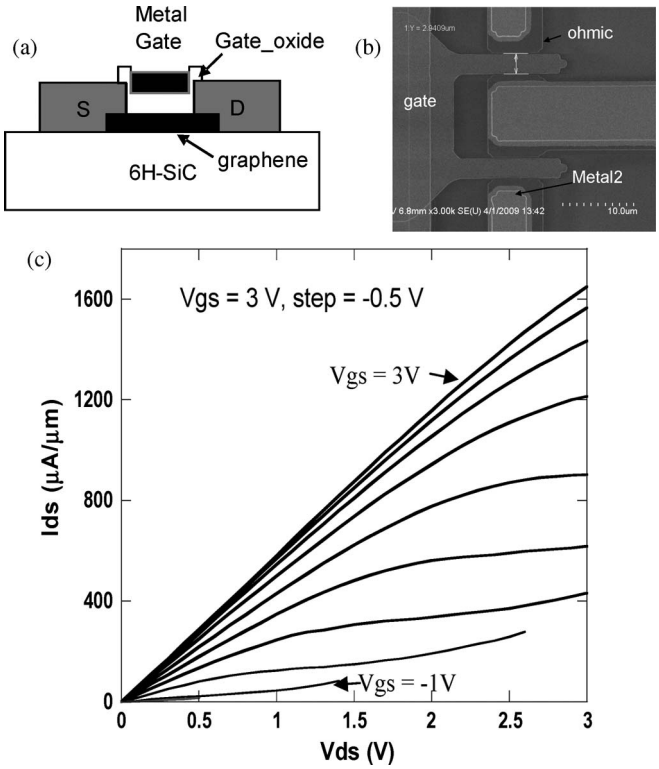

Fig. 1. (a) Schematic of the top-gated graphene FET. (b) SEM photograph of 2f $\times$ 4 μm graphene FET. (c) Measured common-source current–voltage characteristics of 1f $\times$ 4 μm graphene FET.

Fig. 1(c) shows measured room-temperature common-source current–voltage characteristics of a two-gatefinger and 4-μm-wide n-channel graphene FET (denoted as 2f $\times$ 4 μm), in which excellent drain current saturation was observed. The source-to-drain voltage $(V_{\rm ds})$ was swept up to 3 V, where the gate-to-source $(V_{\rm gs})$ voltage was stepped from 3 V (top curve) in steps of -0.5 V. At $V_{\rm ds} = 1$ V, the ON-state current at $V_{\rm gs} = 3$ V was 0.59 A/mm. The OFF-state current was 0.047 A/mm at $V_{\rm gs} = -1$ V, yielding an $I_{\rm on}/I_{\rm off}$ ratio of 12.5. At $V_{\rm ds} = 0.5$ V, the $I_{\rm on}/I_{\rm off}$ ratio increased to 19 with the ON-state current of 0.31 A/mm. At $V_{\rm ds} = 3$ V, the ON-state current at $V_{\rm gs} = 3$ V was measured as high as 1.65 A/mm. The on-resistance was 1.6 $\Omega \cdot$ mm.

Fig. 2 shows the measured transconductance (g_m) of a 2f $\times$ 4 μm graphene FET at different $V_{\rm ds}$, stepping from 1.05 to 3.05 V with a step of 0.5 V. The inset shows measured transfer curves. At $V_{\rm ds} = 3.05$ V, the $I_{\rm ds}$ reached up to 1.1 A/mm at $V_{\rm gs} = 3$ V. The ambipolar behavior was observed clearly at $V_{\rm ds} > 2$ V, while the ambipolar behavior is not well developed with a relatively flat region observed at low $V_{\rm ds}$ such as $V_{\rm ds} =$ 1.05 V. The peak extrinsic g_m of 600 mS/mm was measured at $V_{\rm ds} = 3.05$ V, which is the highest ever, compared with reported values of 1.4 mS/mm [5] and 140 mS/mm [7]. The observed negative transconductance is due to a conversion of n-channel to p-channel.

Fig. 3 shows the transfer curves of six 1f $\times$ 4 μm graphene FETs measured at $V_{\rm ds} = 50$ mV from two different wafers, along with the gate leakage current on the order of $<$ 50 pA. In general, the ambipolar behavior was observed with n-channel operation of the graphene FETs at $V_{\rm gs} = 0$ V. The p-channel

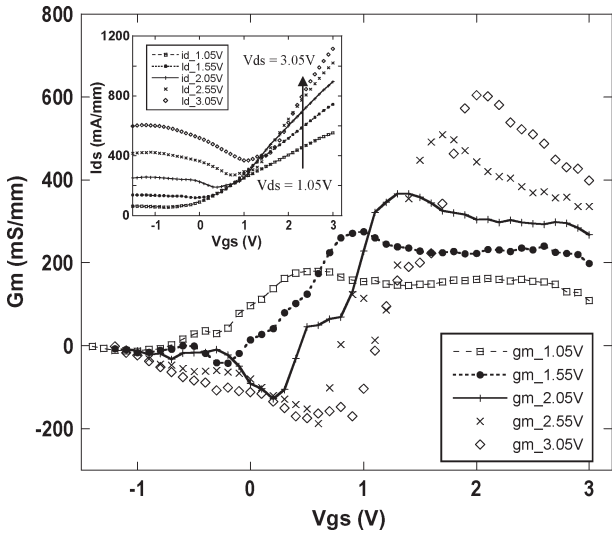

Fig. 2. Measured small-signal transconductance of 1f $\times$ 4 μm n-channel graphene FET at different $V_{\rm ds}$, from 1.05 to 3.05 V in steps of 0.5 V. Peak extrinsic transconductance is as high as 600 mS/mm at $V_{\rm ds} = 3.05$ V. The inset shows measured transfer curves from 1.05 to 3.05 V in steps of 0.5 V.

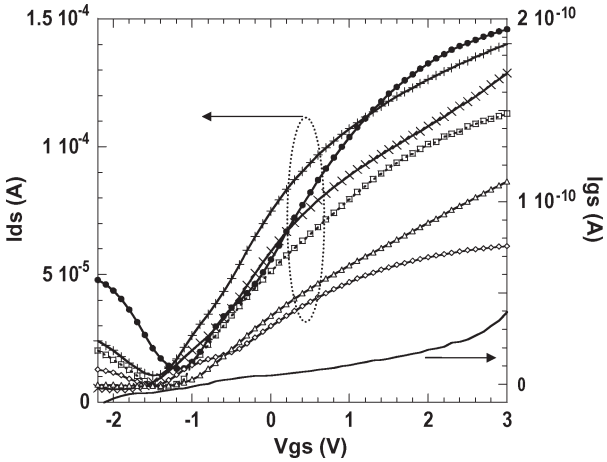

Fig. 3. Measured transfer curves of 1f $\times$ 4 μm top-gated epitaxial graphene FETs at $V_{\rm ds} = 50$ mV. A representative gate leakage current at $V_{\rm ds} = 50$ mV is shown. The $I_{\rm on}/I_{\rm off}$ ratios are 11, 13, 25, 19, 14, and 9.

behavior was observed with threshold voltages (V_T) of -1.5 to -1.35 V, where V_T was set to be a Dirac point for an extraction of the effective mobility for graphene FETs.

Effective mobility $\mu_{\rm eff}$ was extracted using the following formula: $\mu_{\rm eff} = (L/W) \cdot I_{\rm ds}/[C_{\rm ox} \cdot (V_{\rm gs} - V_T) \cdot V_{\rm ds}]$ [10]. In the case of a finite charge density $Q_{\rm Dirac}$ at Dirac point, $\mu_{\rm eff}$ can be corrected accordingly.[1] $C_{\rm ox}$ is the gate oxide capacitance, and $\varepsilon_0 \cdot \varepsilon_{\rm ox}/t_{\rm ox}$, where ε_0 and $\varepsilon_{\rm ox}$ is permittivity of the free space and gate oxide layer, respectively. The gate oxide capacitance is measured using a metal–oxide–metal (MOM) capacitor array with OPEN and SHORT calibration standards. The geometric scaling of the MOM capacitors is verified to eliminate fringe capacitances. The geometric oxide capacitances were measured to be 1 or 1.7 fF/μm^2 from two different wafers. The dielectric constant of the deposited SiO_2 films was determined

[1]In graphene, the effective mobility can be defined as $\mu_{\rm eff} = (L/W) \cdot I_{\rm ds}/[(C_{\rm ox} \cdot (V_{\rm gs} - V_T) + Q_{\rm Dirac}) \cdot V_{\rm ds}]$. This could lead to about 10% correction in $\mu_{\rm eff}$, but not in $\mu_{\rm FE}$, compared to the values in the main text.

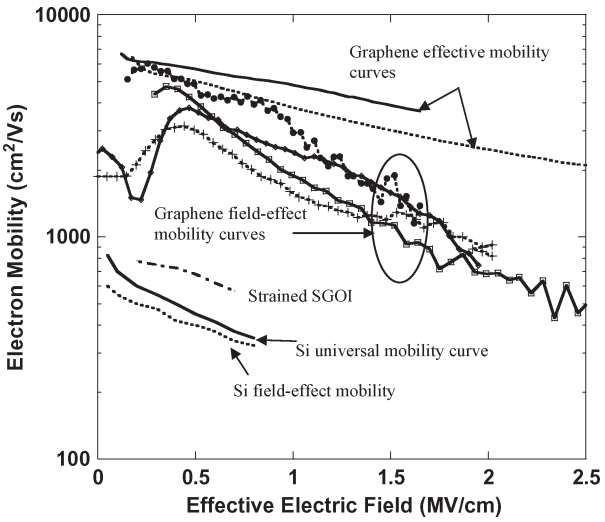

Fig. 4. Measured effective carrier mobility and field-effect mobility of graphene n-FETs are shown in comparison with those of Si n-MOSFET and strained Si on SGOI MOSFET.

to be 3.9, which is close to that of SiO_2. The field-effect mobility $\mu_{\rm FE}$ defined by $\mu_{\rm FE} = (L/W) \cdot g_m/(C_{\rm ox} \cdot V_{\rm ds})$ [10] was obtained from the transconductance (g_m) at $V_{\rm ds} = 50$ mV. Therefore, there is no ambiguity in $\mu_{\rm FE}$ associated with V_T, unlike the case of $\mu_{\rm eff}$. The effective electric field is estimated using $E_{\rm eff} = Q_{\rm Gr}/(\varepsilon_0 \cdot \varepsilon_{\rm ox})$, where $Q_{\rm Gr}$ is the total charge in the graphene channel.

Fig. 4 shows the extracted $\mu_{\rm eff}$ and $\mu_{\rm FE}$ of graphene n-FETs versus the effective electric field $E_{\rm eff}$. For comparison, the universal and field-effect mobilities of Si n-MOSFETs [11] and strained Si n-MOSFETs on SiGe-on-oxide [12] are shown. While both $\mu_{\rm eff}$ and $\mu_{\rm FE}$ of the graphene n-FETs depend on $E_{\rm eff}$, both values were higher than 1000 $\rm cm^2/V \cdot s$ over a wide range of effective electric field up to 1.6 MV/cm. The peak field-effect mobility values ranged from 3200 to 6000 $\rm cm^2/V \cdot s$ depending on the devices shown in Fig. 3. A record field-effect mobility of 6000 $\rm cm^2/V \cdot s$ was obtained at an effective electric field of 0.27 MV/cm from the device (□) shown in Fig. 3. To compare with the measured Hall mobility, which was measured at high carrier concentrations, both $\mu_{\rm eff}$ and $\mu_{\rm FE}$ curves versus $E_{\rm eff}$ were extrapolated using $\mu_{\rm eff} = 6806 \times E^{-0.36E_{\rm eff}}$ for $C_{\rm ox}$ of 1 $\rm fF/\mu m^2$ and $\mu_{\rm eff} = 6111 \times E^{-0.44E_{\rm eff}}$ for $C_{\rm ox}$ of 1.7 $\rm fF/\mu m^2$. At the Hall carrier density of $(9-10) \times 10^{12}/\rm cm^2$, the $\mu_{\rm eff}$ values were extrapolated to be 1120 $\rm cm^2/V \cdot s$ for $C_{\rm ox}$ of 1 $\rm fF/\mu m^2$ and 670 $\rm cm^2/V \cdot s$ for $C_{\rm ox}$ of 1.7 $\rm fF/\mu m^2$. The extrapolated effective mobility values were close to the measured Hall mobility. On the other hand, the $\mu_{\rm FE}$ was extrapolated to be $\sim$50 $\rm cm^2/V \cdot s$ at the Hall carrier density of $(9-10) \times 10^{12}/\rm cm^2$. This is much lower than the measured Hall mobility of $\sim$1192 $\rm cm^2/V \cdot s$. The measured field-effect mobilities of graphene n-FETs were at least seven times higher than that of ITRS Si n-MOSFETs and $\sim$80 times higher than that of ultra-thin-body SOI n-MOSFETs. The peak field-effect mobility of graphene p-FETs was also determined to be 3200 $\rm cm^2/V \cdot s$ at an effective electric field of 0.2 MV/cm.

While more studies are needed for quantitative analysis, the observed excellent I–V saturation, high $I_{\rm on}/I_{\rm off}$ ratio, and high transconductance may be attributed to several factors, including the low source access resistance of $< 0.2\ \Omega \cdot \rm mm$ and the low trapped charge density. The capacitance–voltage measurement of the top-gate metal–SiO_2–graphene diodes was carried out, and the trapped charge density of the SiO_2 layer was estimated to be $\sim 2 \times 10^{11}/\rm cm^2$, which improves the graphene channel mobility and, consequently, g_m. The improvement of the $I_{\rm on}/I_{\rm off}$ ratio may be due to a reduction in charge inhomogeneity near the Dirac point or a formation of a pinch-off region in a zero-bandgap graphene film [13]. We note that the possibility of a small bandgap associated with strained epitaxial graphene film is not excluded. We also note that the peak extrinsic g_m of 600 mS/mm per unit gate capacitance of 1 $\rm fF/\mu m^2$ yields a calculated gate delay of 2 $\rm ps/\mu m$.

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